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Processing of Foturan® glass ceramic substrates for micro-solid oxide fuel cells

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Abstract

The microfabrication of Foturan® glass ceramic as a potential substrate material for micro-solid oxide fuel cells (micro-SOFC) was investigated. Foturan® was etched in 10% aqueous hydrofluoric (HF) acid solution at 25 °C with a linear rate of 22 ± 1.7 μm/min to create structures with an aspect ratio of 1:1 in 500 μm-thick Foturan® substrates for micro-SOFCs. The concentration of the HF etchant was found to influence the etching rate, whereas the UV-exposure time creating nuclei in the glass for subsequent crystallization of the amorphous Foturan® material had no significant influence on the etching rates. The surface roughness of the crystallized Foturan® was determined by the crystallite size in the order of 10–15 μm. Free-standing micro-SOFC membranes consisting of a thin film Pt cathode, an yttria-stabilized-zirconia electrolyte and a Pt anode were released by HF etching of the Foturan® substrate. An open-circuit voltage of 0.57 V and a maximum power density of 209 mW/cm^2 at 550 °C were achieved.

Keywords: Foturan®; Photostructurable glass ceramic; HF etching; Micro-solid oxide fuel cell; Micro device

1. Introduction

The demand for micro-electro-mechanical-systems (MEMS) and micro-electro-ceramic-systems (MECS) with short response times and high functionality has increased in the last years. Microfabricated planar micro-solid oxide fuel cell (micro-SOFC) systems are considered as promising battery replacements due to their high energy density and specific energy.[1–3] The heart of these micro-SOFC systems consists of a less than 1 μm thin free-standing ionic-conducting ceramic membrane that is integrated on a microstructurable substrate.[2,4–16] Up till now, the integration of micro-SOFC membranes in portable electronics is still under investigation. Recently, the proof-of-concept for such micro-SOFC membranes based on thin film technologies and microfabrication was demonstrated by several research groups.[2,4–16]

Possible substrates for micro-SOFC membranes are silicon or glass ceramic such as Foturan®. The former approach is adopted from typical silicon processing and was used to support free-standing micro-SOFC membranes.[4,13–16] The latter approach is based on direct structuring of Foturan® which is a photosensitive Li_2O–Al_2O_3–SiO_2 glass ceramic.[2,12]

Foturan® glass can be structured for a variety of purposes. This material combines the properties of glass and the opportunity to achieve very fine structures with tight tolerances and high aspect ratios (hole depth/hole width) by chemical etching. The Foturan® surface is masked and exposed to UV light in order to initiate seeds in the glass for the later crystallization by thermal treatment. During the subsequent annealing in the temperature range of 500–600 °C, the nuclei in the UV-exposed areas initiate crystallization of the glass. The crystalline regions, when etched with a 10% aqueous HF acid solution at room temperature, have an etching rate up to 20 times higher than that of the vitreous regions.[17–19] The advantage of a glass-ceramic substrate for the fabrication of a support for micro-SOFC membranes is its thermal expansion coefficient of $\alpha = 10.6 \times 10^{-6}\,K^{-1}$ (at 20 °C)[20] which is very close to that of the oxygen ionic-conducting ceramic thin films such as yttria stabilized zirconia with $\alpha = 10.8 \times 10^{-6}\,K^{-1}$ (between 20 °C and 800 °C).[21] The electrical resistivity of crystallized Foturan®

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is $5.6 \times 10^{16}\,\Omega\,cm^{-2}$ [22] and, thus, Foturan® is electrically insulating.

The literature reports about the fabrication of holes, pits, cavities or channels with Foturan® substrates for applications such as micro fluidics, mechanics, optical and micro-total analysis systems (micro-TAS) applications.[23,24] The fabrication of free-standing membranes on Foturan® substrates was reported for the first time by Muecke et al. for the application of a micro-SOFC membrane.[12]

For the fabrication of free-standing membranes deposited on Foturan®, the exact etching times have to be known in order to avoid contact of the membrane with the etchant. A possible attack of adjacent layers during HF etching of Foturan® at 25 °C is discussed with respect to microstructural changes and the impact on the electrical conductivity in Refs. 25,26. It was found that the microstructures of gadolinia-doped-ceria thin films were attacked by HF, whereby the less crystalline films are more seriously affected. The electrical conductivity of the thin films becomes smaller due to contact with HF, but does not break down.[25,26] Kossoy et al. reported that yttria-stabilized-zirconia thin films are resistive toward HF attack.[27]

Dietrich et al. reported an etching rate of 10 μm/min for Foturan® structures larger than 500 μm in 10% HF. The minimal achieved feature size was holes with a diameter of 25 μm and a hole depth of 75–200 μm. Smaller feature sizes were not possible due to the size of the Foturan® crystals of about 10 μm which are formed during crystallization of the Foturan®. The authors point out that the minimum achievable hole diameter depends on the thickness of the substrate or the depth of the required structure.[18] Hülsenberg and Bruntsch reported on the tolerance of the size of holes etched into Foturan® wafers with different thicknesses.[28] They reported smallest achievable holes of 120 μm in diameter etched into plates with a thickness between 500 μm and 1 mm.[28] An etching depth of 0.4 mm after 8 min was observed with the use of an ultrasonic etching bath. For the same time without ultrasonication, the etching depth was only 0.15 mm.[29] Brokmann reported an etching rate for a feature size of 100 μm in diameter and a substrate thickness of 700 μm in an ultrasonic etching bath with 10% HF. The etching rate of 28 μm/min was determined for etching times between 1 and 4 min.[30] During the first minutes of wet etching of a 1 mm thick Foturan® substrate in 5% HF, Stillman et al.[31] found an average etching rate of 18.7 ± 2.2 μm/min for pit widths of 10–1280 μm for the first 3 min of etching. In a second experiment under the same conditions, a few plates with different outline widths could be released after 30 min, and all plates were released after 60 min. The authors expected the plates to be released after 27 min calculated from the maximum etching rate. The reason for the variation in the etching rates was due to a chemically inhomogeneous base material as well as the variation in the laser power from pulse to pulse in their experiments.[31]

In summary, Foturan® glass ceramic is a substrate material for the fabrication of holes or cavities with etching rates from 10 to 28 μm/min depending on the use of ultrasonication of the etchant concentration and the substrate exposure time.[18,28,31,32]

On the other hand, it was also reported that both, silicon and Foturan® are promising substrate candidates for fabricating power-delivering free-standing micro-SOFC membranes.[12,16] However, it is still unclear whether silicon or Foturan® glass ceramic is the best substrate material choice for this application, since both substrate materials have advantages and disadvantages with respect to SOFC application. Foturan needs high temperature annealing processes, which might damage thin films, it requires HF etching and it is known to be not fully homogeneous. Silicon, on the other side is electrically not insulating, it is not transparent and has a very different thermal expansion coefficient compared to the functional thin films used in the micro-SOFC membrane.

In this work, we thus studied in detail the processing of Foturan® glass ceramic with the aim of fabricating power delivering free-standing micro-SOFC membranes. Foturan® wafers are characterized and the influence of the wafer thickness, aspect ratio, UV-exposure time and etchant concentration on the etching characteristics is investigated. The fabrication of free-standing membranes on Foturan® substrates is critically discussed.

2. Experimental

All experiments were carried out on 4-in. Foturan® wafers with thickness of 250 μm and 500 μm provided by Mikroglas, Chemtech, Mainz, Germany.

2.1. Etching of the Foturan® substrate

The double-side polished, amorphous Foturan® substrates were covered by a 30 nm thick Cr adhesion layer and a 100 nm thick platinum layer with circular holes of 200 μm in diameter by sputtering. The Cr/Pt film is a hard mask acting as a protective layer during UV exposure. Both layers were deposited with a custom-made RF sputtering tool with 100 W, 3×10^{-3} mbar base pressure, 80 mm working distance through a 0.3 mm thick stainless steel mask and a working pressure of 2×10^{-3} mbar Ar. After deposition of the Cr/Pt layer, the wafer was irradiated using UV light (Electronic Visions Group AL 6-2, 312 nm, 500 W) for 1 h and 2 h, respectively at a distance of 5 cm. The Foturan® wafer was then cut with a dicing saw (Disco DAD 321, Tokyo, Japan) into 2.5 cm × 2.5 cm chips. For crystallization, the irradiated Foturan® chips were sandwiched between two alumina plates in order to avoid warping during annealing in air (Nabertherm controller P320, Lilienthal, Germany). Annealing was performed at a heating and cooling rate of 1 °C/min up to 500 °C and 600 °C with a dwell time at the highest temperatures of 2 h for complete crystallization of the UV-exposed Foturan®. The wafer piece was then covered by a HF protective photo resist coating (FSC-H, Rohm and Haas, Coventry, UK) on the Cr/Pt side in order to prevent double side etching. For this, the chip was first pre-baked on a hotplate at 120 °C for 30 min in order to remove adsorbed species and then the HF protective coating was brushed over the whole chip surface, followed by a post bake at 100 °C for 45 min on the hotplate.

For wet etching, the Foturan® chips were mounted horizontally in a custom made etch bath. In order to determine the wet

etching rate as function of the etchant concentration, a 2% and a 10% HF solution in water (diluted from 40% HF, Suprapur, Merck, Germany) were prepared. The etching was carried out under constant stirring for different lengths of time between 4 and 30 min at 25 °C. After wet etching the HF protective coating was removed with acetone. The etching depth of the etched hole was determined on fractured cross sections of the chips by scanning electron microscopy (SEM, Leo 1530, Carl Zeiss, Germany) focusing perpendicular to the hole. The accuracy of the depth of the etched hole was ±15 μm due to the grain size of the Li_2SiO_3 dendrite crystals in the illuminated regions of the partially crystallized material after annealing.

In order to characterize the surface roughness of etched Foturan® wafer, a complete 4-in. 500 μm thick, double-side polished wafer was exposed to UV light with a wavelength of 312 nm and annealed as described previously for the crystallization. The whole 4-in. wafer was etched in a stirring 10% aqueous HF solution for 3 min as described above at 25 °C. A surface z-profile tester (Hommel T 1000, Jenoptic, Jena, Germany) was used for topography mapping of the etched surface on several positions on the 4 in. wafer.

2.2. Micro-solid oxide fuel cell fabrication

The experimental steps for the fabrication of the micro-SOFC on a Foturan® substrate are explained in detail elsewhere.[12] The deposition of Pt/Cr current collector onto the Foturan® wafer and the exposure to UV light were performed as described above. The deposition condition of the micro-SOFC thin films on the Foturan® wafer piece are performed according to Muecke et al.[12]

2.2.1. Platinum electrodes deposition

The Pt thin film for the anode was deposited on top of the Pt/Cr current collector by sputtering (SCD 050, Balzers, Liechtenstein) at room temperature with an argon pressure of 0.05 mbar, a sputter current of 60 mA and a sputter time of 5 min resulted in a film thickness of 100 nm. The Pt thin film cathode was deposited with the same parameters on top of the electrolyte layer.

2.2.2. Yttria stabilized zirconia electrolyte deposition

The bilayer 8 mol.% yttria-stabilized-zirconia (8YSZ) electrolyte thin films were deposited by two different methods on top of the Pt anode. The bottom 8YSZ thin film layer was deposited by pulsed laser deposition (PLD, surface PLD workstation, Hückelhoven, Germany) from a sintered $(Y_2O_3)_{0.08}(ZrO_2)_{0.92}$ target with an 248 nm excimer laser (laser-fluence: 4 J/cm^2, pulses: 54,000, rate: 10 Hz). The 300 nm thick 8YSZ thin films were deposited through a chromium mask at a substrate–target distance of 8.5 cm, a substrate temperature of 400 °C and an oxygen chamber pressure of 2.66 Pa.[12] In order to prevent gas-leakage through this 8YSZ electrolyte layer deposited by PLD, an additional 8YSZ layer was deposited by spray pyrolysis on top to seal off the eventual pores or pinholes. An 8YSZ precursor solution is vaporized at an air pressure of 1 bar and a feed rate of 5 mL/h. The precursor had a salt concentration of 0.05 mol/L consisting of zirconium acetylacetonate (Fluka, 96% purity) and yttrium chloride hexahydrate (Alfa Aesar, 99.9% purity) dissolved in 80:20:20 vol.% of tetraethylene glycol (Aldrich, 99% purity):polyethylene 600 (Fluka, purum):ethanol (Fluka, purum, 99.8%). The Foturan® substrate temperature was 410 °C and the spray time was set to 90 min resulting in a film thickness of 300 nm. The thin films were covered with a protective coating during the etching of Foturan® to release the micro-SOFC membranes. The contacting of the micro-SOFC electrodes was performed via flat-pressed 80 μm Pt wires as explained in detail elsewhere.[12]

2.3. Micro fuel cell membrane characterization

Electrochemical testing of the micro-SOFC chips was carried out between 400 °C and 550 °C, under air (cathode) and 3 vol.% humidified N_2:H_2 4:1 (anode). All gas flows (60–500 sccm) were controlled by mass flow controllers (El-Flow, Bronkhorst, Switzerland). The heating and cooling rates were 3 °C/min. Current–voltage curves were recorded with an IM6 workstation (Zahner Elektrik, Germany) at the open-circuit voltage (OCV). The data was normalized to the area of the free-standing micro-SOFC membrane.

3. Results and discussion

3.1. Foturan® wafer characteristics

The 4-in. Foturan® wafers were characterized by comparing as-delivered wafers from the same batches with respect to optical appearance and surface topography. The as-delivered wafers are amorphous and transparent. After exposure to UV light and subsequent annealing at 600 °C for 2 h, the wafers crystallize and turn brownish (Fig. 1(a) and (c)). Strong glass streaks with color changes between white and brown are visible for the wafer in Fig. 1(a). The wafer as shown in Fig. 1(c) shows mainly brownish colors with fewer white streaks after annealing. After 3 min wet etching in 10% diluted HF solution at 25 °C, the color of the surfaces turns white for both wafers. Different amounts of strong white glass streaks are distributed in different locations on the surfaces; mainly the pattern from the annealed, but non-etched material is visible (Fig. 1(b) and (d)). Below the surface, the brownish bulk material is visible. For the wafer presented in Fig. 1(a) and (b), the white glass streaks are visible on the same wafer position before and after etching. For the second wafer, the white glass streaks seem to be different before and after etching (Fig. 1(c) and (d)). The reason might be that the glass streaks are deeper in the bulk material after annealing and therefore less pronounced in digital imaging.

The surface profiles, measured in the red-marked areas (Fig. 1(b) and (d)) on the two Foturan® wafers (taken from different batches and microstructured under same conditions), are presented in Fig. 2. Height differences from 15 to 20 μm are found and can be correlated to the colors of the wafer and the grain size of the material. The strong white areas represent the maximum heights and the brownish zones correlate with the minimum heights. From these results we have to conclude that two wafers from the same delivery batch are etched inhomogeneously. We ascribe these height differences combined with the

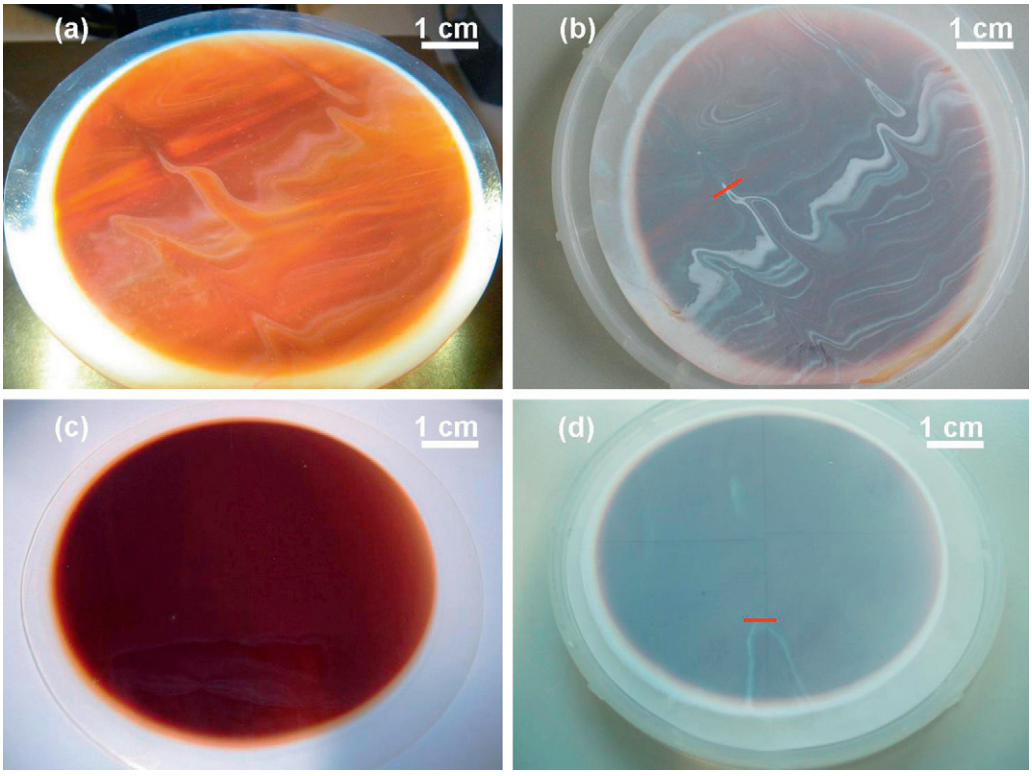

Fig. 1. Light photographs of two 4-in. Foturan® wafers from the same batch after UV exposure of 2 h and annealing at 600 °C for 2 h (a and c). The same wafers are shown after wet etching for 3 min in 10% HF at 25 °C (b and d). The red marked areas in (b) and (d) correspond to the measured areas for the surface roughness shown in Fig. 2. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of the article.)

streaks, which are optically visible (Fig. 1) to small variations in the chemical composition in the glass melt (probably of the seeds for crystallization) of the glass wafer within one batch prior to the etching. These differences in the chemical composition affect the degree of crystallinity of the wafer after UV-light exposure and annealing. Evans et al. reported that the colors of the Foturan® reflect different nucleation and crystallization states.[33] Transparent colors indicate amorphous and dark brown areas biphasic amorphous–crystalline to fully crystalline microstructures. As it is known that the glass is etched 20–30 times slower compared to the fully crystalline material,[18] it is consistent that the white areas of the wafer are higher, and therefore less etched than the brownish areas. These differences in etching behavior are found in the centimeter range on the 4-in. wafer. As a consequence, differences in etching rates have to be expected if one aims at making arrays of equal sized hole depths. Hence, it becomes difficult to etch geometrically identical small features over large areas in a Foturan® wafer.

In Fig. 3, a SEM cross-sectional view of the sidewall of an etched hole in the crystallized Foturan® is shown. It shows a rough surface and some holes in the structure (dark areas) as well as dendritic Li_2SiO_3 grains forming tree-like branches of 8–10 μm in diameter in the planar view (2D) (white circles in Fig. 3). In 3D, the crystals are as large as 12–15 μm and are

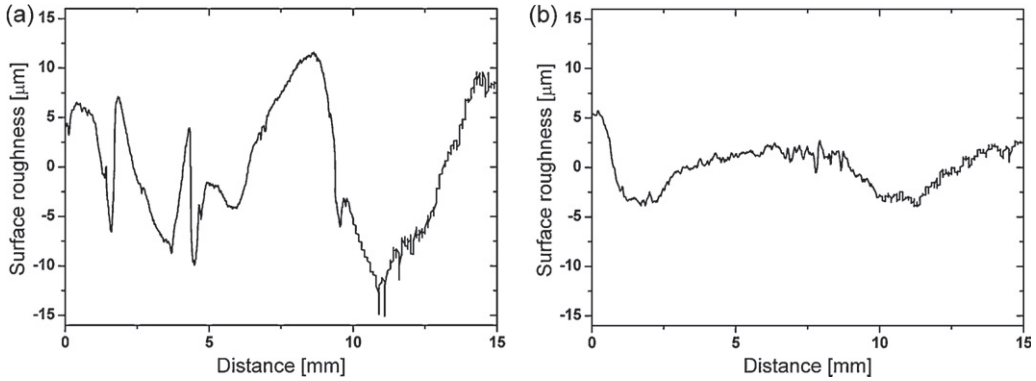

Fig. 2. Foturan® surface roughness profiles after 3 min etching in 10% HF at 25 °C: (a) surface roughness profile corresponding to the red line in Fig. 1(b); (b) surface roughness profile corresponding to the red line in Fig. 1(d).

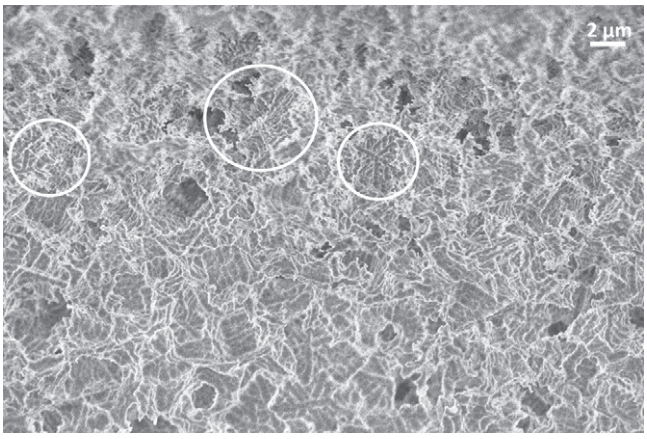

Fig. 3. SEM cross-sectional image of the sidewall of a Foturan® hole after etching for 15 min in 10% HF at 25 °C. Microstructure with dendrite Li_2SiO_3 grains forming tree-like branches of 8–10 µm in diameter in the planar view (circles).

formed by hexagonal crystalline platelets that form a continuous path in three dimensions and allow the glass-ceramic to be etched with hydrofluoric acid, which attacks the low-silica crystallites at a far greater rate than the durable aluminosilicate residual glass as already described by Beall.[34]

3.2. Wet etching rates of Foturan®

In order to elucidate the influence of substrate thickness versus hole diameter on the etching rate, the UV-exposure time and etchant concentrations were varied in etching holes of different diameters (∅ = 200–500 µm) in wafers of 250 and 500 µm thickness. The hole depths were measured after different etching times by scanning electron microscopy. The results are shown in Fig. 4. The error bars indicate the deviations from the mean value of three individual hole depths on the same chip (2.5 cm × 2.5 cm) etched under identical experimental conditions.

For all conditions with 10% aqueous HF acid solutions, constant etching rates of 21–25 µm/min were found up to an etching depth of 300–350 µm. For larger hole depths progressively lower etching rates were obtained, and with it, a deviation from the linear behavior. The accuracy of ±2.5 µm is due to the error in the determination of the etching depth.

The influence of the substrate thickness on the etching is presented in Fig. 4(a). For a 500 µm thick wafer with a 500 µm hole (aspect ratio of 1:1), the etching rate was 21 ± 2.5 µm/min (Fig. 4(a); circles) in the linear regime. After 23 min, a 500 µm deep hole was etched into the Foturan®. This finding is reproduced also using thinner wafers (250 µm) and the small hole diameter (∅ = 200 µm) resulting in an aspect ratio of 2.5:1 (Fig. 4(a); filled symbols). In the case of a smaller hole diameter (∅ = 200 µm) and a Foturan® thickness of 500 µm, a constant etching of 22 ± 1.7 µm/min up to 300 µm was found. Mass transport limitation of the fresh HF etchant to the etching front results in a lower etching rate at larger depths than 300 µm with the consequence that 31 min are required for etching the hole (Fig. 4(a)), square symbols. This is in fair agreement with results of Beckel et al. who reported an etching time of 27 min for the same wafer thickness.[35]

The exposure time to UV light is an important parameter for generating crystallization seeds throughout the entire wafer thickness and for a complete crystallization of the Foturan® wafer. Therefore several Foturan® chips with a thickness of 500 µm and a hole diameter of 200 µm were exposed to UV light for 1 h and 2 h, respectively. The etching depth versus time is shown in Fig. 4(b). For both exposure times an etching rate of around 22 µm/min was found. The slowdown of the etching rate at larger depths than 300 µm is again due to mass transport limitation. This indicates that an UV irradiation of 1 h is enough to reach the saturation regime found by Livingston et al. to induce the maximum nuclei seeds throughout the entire cross section.[36]

The here reported etching rates of ∼22 µm/min are 20–50% larger than the etching rates of 10–18 µm/min reported previously in the literature.[18,25,27,28,32] This might be related to differences in the average grain size, mainly determined by the nuclei concentration, the annealing temperature and time of the Foturan® and to the stirring conditions in the etching bath. Evans et al. investigated the crystallization on the present Foturan® wafer batches and reported a primary average grain size of 2–5 µm for crystallization at annealing temperatures below 700 °C and a second crystallization process for higher temperatures (820 °C) resulting in a secondary grain formation with 100–200 nm grain size in average.[33] However, these 2–5 µm grains join forming tree-like dendrite grains as large as 12–18 µm. Previous investigations on etching rates in the literature were performed on Foturan® with grain sizes of about 1–10 µm[18] with reported etching rates of 10 µm/min. Most researchers use a one-step annealing process with 1 h dwell at 500 °C[18], 560 °C[24] resulting in grain sizes of 3–5 µm. Livingston et al. investigated the microstructure of irradiated and annealed Foturan® and found Li_2SiO_3 grain sizes to range between 0.7 and 1.0 µm after annealing at 607 °C for 1 h. At high light fluences (laser powers exceeding 15 mW) they reported saturation and no dependence of etching rate from the light intensity and an etch rate of the irradiated material of 18.6 µm/min.[36] Stillman et al. used a two-step annealing process of 1 h at 505 °C followed by 1 h at 605 °C to fully crystallize the Foturan® substrate without reporting the grain size.[37] This is close to the annealing process used in this work using a heating and cooling rate of 1 °C/min up to 500 °C and 600 °C with a dwell time at the highest temperatures of 2 h to complete the crystallization of the UV-exposed Foturan®.

Based on the reported annealing conditions and etching rates, it can be concluded that the Foturan® can be etched very fast in 10% HF at 25 °C and rapid fabrication of cavities or holes with feature sizes in the range of lateral dimensions of 100–500 µm are therefore possible with depths of 200–500 µm. However, the etch stop at the 8YSZ membrane might be a problem for the fabrication of free-standing micro-SOFC membranes with an etching rate of 22 µm/min in 10% HF, which means that five layers of dendrite Li_2SiO_3 grains forming tree-like branches are etched in only 30 s. Therefore, the handling of the etching process during microfabrication has to be very accurate, because the adjacent functional 8YSZ layers can easily be

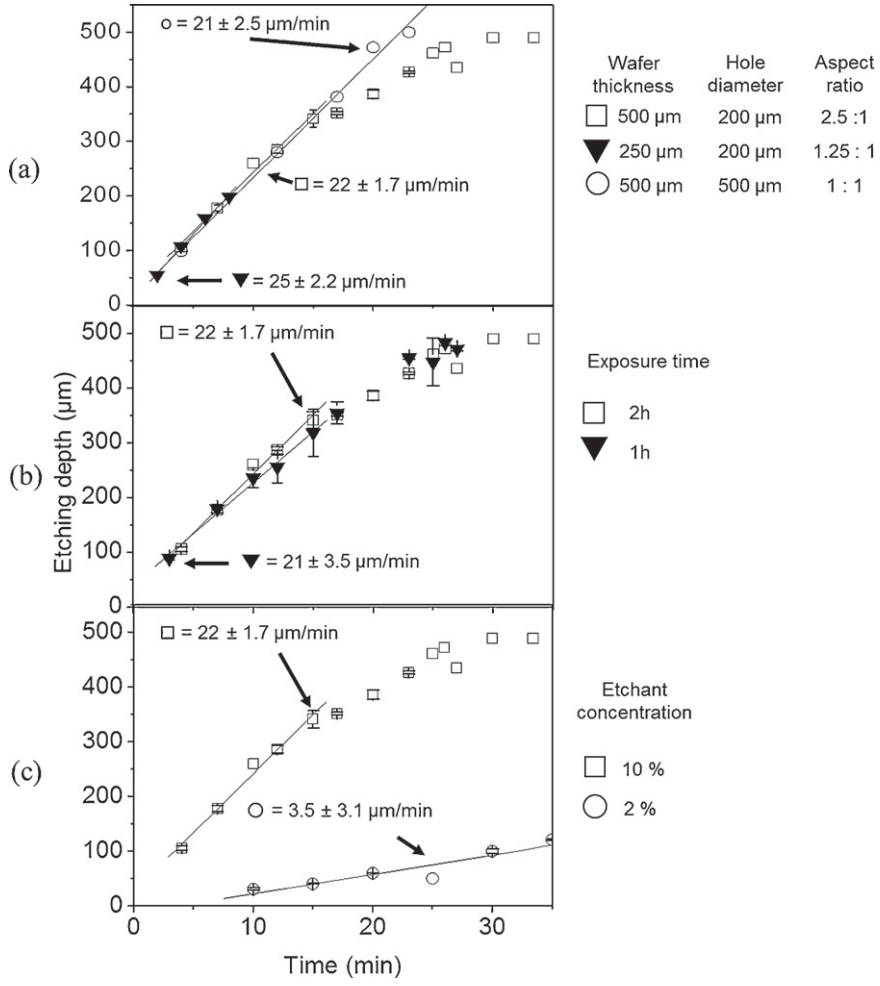

Fig. 4. Depths of etched holes in Foturan® as function of substrate thickness and hole diameter (a), UV-exposure time (b) and HF etchant concentration (c). The results in (b) and (c) are based on holes of 200 µm diameter. The relative error was calculated from the differences of three individual etching depth values on one chip for each point of time. Errors are only given, when three data points were measured.

attacked.[18,24,26,30,38] For this reason, the etching rate for a lower concentrated aqueous HF acid solution at 25 °C was also investigated. The wet etching rates are shown for the example of a 2% HF etchant in Fig. 4(c) and found to be 3.5 ± 3.1 µm/min. This is a reduction by a factor of 6.5 compared to 10% HF. The influence of the substrate thickness for the lower concentrated aqueous HF solution was not investigated. Nevertheless a constant etching was found up to a substrate thickness of 250 µm. In order to avoid an attack of deposited 8YSZ thin films of the free-standing membrane by the HF etchant, it is recommended to use a lower concentration of the HF solution.

In summary, it is possible to etch holes with an aspect ratio of 1:1 into 500 µm thick Foturan® wafers with a constant etching rate through the entire thickness of the wafer. For higher aspect ratios, mass transport limitation of fresh HF etchant to the etch front results in lower etching rates at depths larger than 300 µm. The etching rates can be adjusted with the concentration of the HF etchant. No influence of the exposure time on the etching rate was found under these UV illumination conditions. The influence of the temperature of the aqueous HF solution was not investigated due to safety reasons.

3.3. Foturan® as a support for micro-SOFC membranes

3.3.1. Hydrofluoric acid etching of the crystalline Foturan® wafer for processing of a micro-SOFC

The wet etching rates of Foturan® determined in the previous section can be applied in order to obtain free-standing micro-SOFC membranes on a Foturan® support. A microfabricated Foturan® chip with three contacted micro-SOFC membranes is shown in Fig. 5(a). A cross-sectional schematic of the free-standing membranes is shown in Fig. 6(b).

The wet etching in 10% hydrofluoric acid of a 200 µm hole from the backside of a 500 µm thick Foturan® wafer to release the <1 µm thin free-standing membranes was carried out for 23 min as determined from Fig. 4. Even for Foturan® chips from the same wafer, three different cases were observed for an etching time of 31 min as depicted schematically in Fig. 6(a)–(c), along with the corresponding SEM cross-sectional images (Fig. 6(d)–(i)) and bottom-view optical micrographs of the free-standing membranes (Fig. 6(j)–(l)). In general, we observed three different situations due to differently etched holes in the Foturan® wafer.

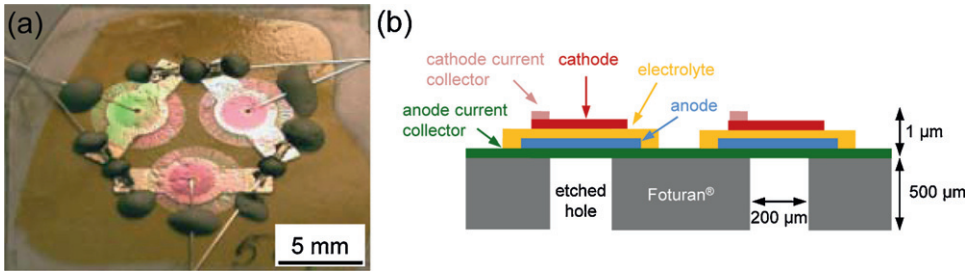

Fig. 5. Photograph of a Foturan® chip with three contacted micro-SOFC membranes (a). Schematic of a cross-section of a Foturan® chip with free-standing micro-SOFC membranes (b).

Fig. 6(a) shows schematically a none-free etched hole. The 8YSZ membranes are still covered with a thin layer of Foturan® at the bottom end of the hole and the thin films are not free-standing (Fig. 6(d) and (g)). The optical microscopy image taken in the transmitted light mode shows that the membranes that are not etched free have a reddish color due to the remaining layer of crystalline Foturan® (Fig. 6(j)).

Fig. 6(b) shows the most frequent case, in which the membranes are etched free, however there are still a few remaining

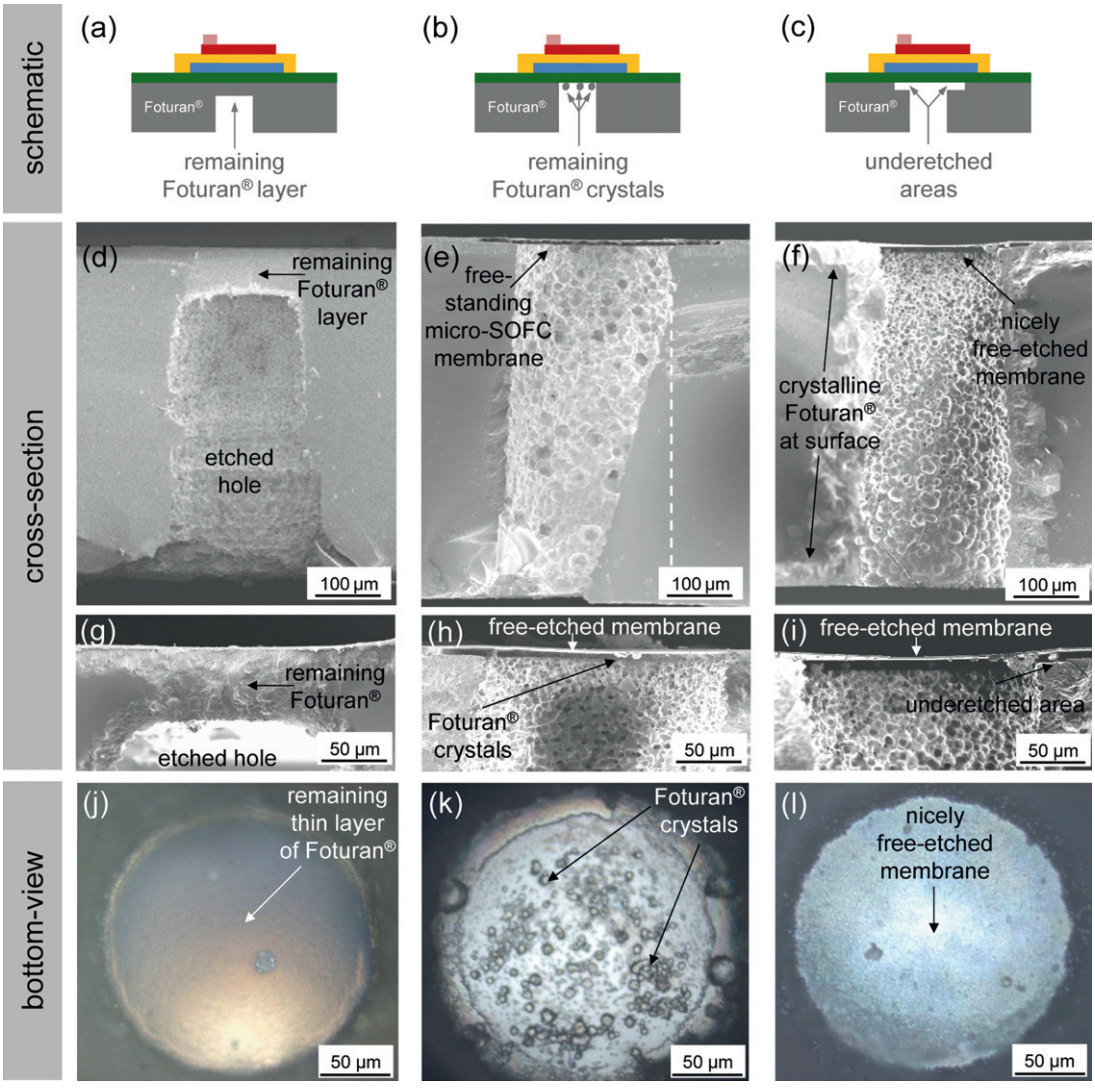

Fig. 6. Cross-sectional schematic of 3 different etching scenarios: not etched free (a), a few remaining Foturan® crystals (b), and free-etched membrane (c). Corresponding scanning electron microscope cross-sectional images of the 200 µm hole etched into the 500 µm thick Foturan® (d–f) and an enlargement of the free-standing membranes (g–i). The dashed line in (e) shows the sidewall of the etched hole, as the Foturan® wafer did not break symmetrically. The corresponding optical microscope images taken with transmitted light looking through the etched hole onto the bottom side of the free-standing membrane for the 3 cases are shown in (j–l).

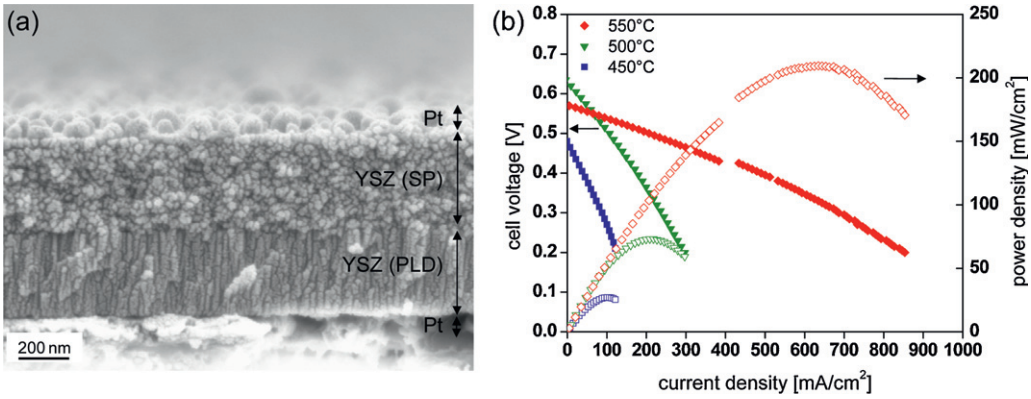

Fig. 7. (a) Scanning electron microscope cross-sectional images of free-standing membranes with a diameter of 200 μm consisting of a bilayer 8 mol.% yttria-stabilized-zirconia (8YSZ) electrolyte deposited alternately by pulsed laser deposition (PLD) and spray pyrolysis (SP), with sputtered Pt electrodes. Current–voltage (filled symbols) and power density (empty symbols) curves of the micro-SOFC with the bilayer electrolyte measured in air (cathode) and humidified N_2:H_2 4:1 (anode).

Foturan® crystals attached to the free-standing membrane (Fig. 6(e), (h) and (k)).

In Fig. 6(c), a completely free-etched membrane is shown. From the in the SEM cross-sectional images (Fig. 6(f) and (i)), it can be seen that the membrane is already slightly underetched at the rim of the hole in the Foturan® as indicated in (Fig. 6(i)). This underetching which occurs at the rim of the substrate and the membrane was also observed by Muecke et al.[12] and is caused by the etching of the crystalline Foturan® that has undergone a metal-induced crystallization in the proximity of the Pt/Cr current collector of the membrane.[12] The etching rate in this underetched geometry is rather low due to very high aspect ratio of the channel and it mainly adds a small additional free surface to the 8YSZ electrolyte membrane. The lighter area on both sides the etched hole in Fig. 6(f) is due to the Foturan® wafer not breaking nicely for the cross-sectional image. The same applies for Fig. 6(e) where there is still some remaining Foturan® covering the bottom right part of the hole (indicated by the dashed line).

3.3.2. *Pt/Cr thin film as an etch-stop at the Foturan 8YSZ electrolyte interface*

The etch stop at the Foturan® wafer – micro-SOFC membrane interface is especially crucial. From microfabrication literature, it is known that conventional metal films such as Pt or Cr serve as etch stops due to their high etch resistance toward 10% HF acid.[39] In this current micro-SOFC design, the Pt/Cr metal current collector deposited onto the Foturan® wafer also acts as the etch-stop layer between the HF acid and the micro-SOFC 8YSZ electrolyte thin film during etching. However, once the Foturan® substrate with the micro-SOFC layers has been heat-treated to temperatures of above 400 °C to crystallize the Foturan®, the Pt/Cr metal films undergo agglomeration.[40–42] Now, the HF acid can attack somewhat the bottom side of the 8YSZ electrolyte thin film (the top side of the 8YSZ is covered by a protective coating). Recent etching studies showed that 10% HF acid damages the microstructure of CeO_2-based electrolyte thin films.[25,26] As the conductivity of the Gd-doped CeO_2 is slightly reduced by the HF acid only after 10 min, it is unclear how strongly the microstructure and the conductivity of the 8YSZ will be influenced by the HF acid.[26] Compared to CeO_2-based films, it is however known that 8YSZ tends to be less affected by HF acid.[27]

3.4. *Fuel cell testing of a micro-SOFC with a bilayer electrolyte*

Foturan® chips with three intact free-standing micro-SOFC membranes (as shown in Fig. 6(a)) were fabricated by etching for 27 min. An exemplarily SEM cross-sectional image of such a free-standing micro-SOFC membrane comprising a bilayer 8YSZ electrolyte deposited by PLD and spray pyrolysis is shown in Fig. 7(a). This 500 nm bilayer electrolyte is expected to be gas-tight, as the columnar microstructure of the 8YSZ (PLD) film is sealed off by the granular microstructure of the 8YSZ (SP) film. The current–voltage and power density characteristics of one membrane on a Foturan® chip consisting of three micro-SOFCs are given in Fig. 7(b). The open circuit voltage is 0.57 V and the maximum power density is 209 mW/cm^2 at 550 °C. These high power density values are also representative for another membrane on the same Foturan® chip. The lower than expected OCV (∼1.1 V) of these cells might be attributed to micro-cracks in the electrolytes due to contact of the electrolyte during HF etching. Despite this non-theoretical OCV we measured a higher power density compared to Muecke et al.[12] The latter is likely due to an improved electrode configuration: here we use two sputtered 80 nm Pt electrodes whereas only one 50 nm sputtered Pt anode and a Pt paste-dot acting as the cathode was used in the work of Ref. 12. The optical microscope images of the three membranes after testing is shown in Fig. 8: two membranes were still intact (Fig. 8(a) and (b)) and one of the membranes was cracked after testing (Fig. 8(c)). Cracking can be caused due to the mechanical force during stirring of the HF solution and crack propagation during thermal treatment. The cracked membranes can explain the non-theoretical OCV that was measured as gas-leakage through this neighboring membrane might have reduced

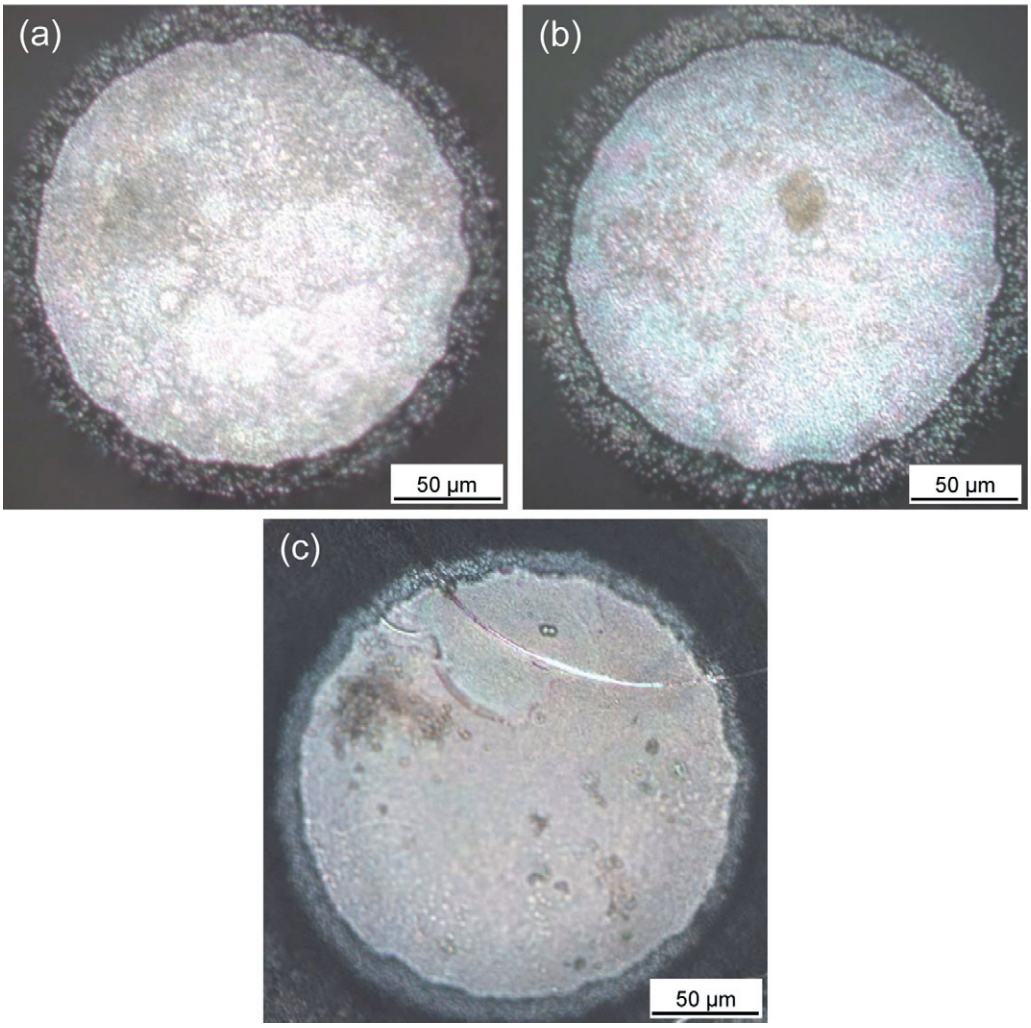

Fig. 8. Optical microscope images taken with transmitted light looking through the etched hole onto the bottom side of the free-standing membrane for three membranes on the same Foturan® chip: (a) and (b) are perfectly free-etched and are still intact after micro-SOFC testing, whereas (c) has a crack after electrochemical testing.

the OCV of the other two membranes. After fuel cell testing at 550 °C for 2 h, the Pt electrodes were agglomerated; especially on the anode side which was exposed to hydrogen. This is in agreement with observations reported in the literature.[40–42]

These results show that it is possible to get good electrochemical performances from individual micro-SOFCs deposited onto a 500 μm thick Foturan® substrate with an etched hole of 200 μm in diameter. The three different cases depicted in Fig. 6, however, show that it is problematic to get reproducibly free-standing membranes on one chip.

4. Summary and conclusion

Foturan® was used as substrate for micro-SOFC elements. The wet etching rate in 10% aqueous HF acid solution at 25 °C as function of substrate thickness, UV-exposure time and etchant concentration for crystallized Foturan® glass ceramic was investigated. Holes of 200 μm in diameter were etched in 200–500 μm thick glass ceramic wafers. Constant etching rates were obtained for aspect ratios of 1:1. For larger aspect ratios, the etching rates decrease due to the mass transport limitation of fresh etchant to the etch front. Etched Foturan® develops a surface roughness of 10–15 μm corresponding to the grain size in the material. After crystallization, different colors of the surface of the wafers indicate different degrees of nucleation and crystallization after exposure and annealing. The preparation of free-standing 8YSZ membranes of 200 μm in diameter and <1 μm thickness on Foturan® by etching was demonstrated. It was also found that chemical inhomogeneities within the Foturan® wafer lead to differences in the etching rates, which is unfavorable regarding a Foturan® chip with multiple micro-SOFC membranes. However precise etching times are required in order to not destroy the deposited thin films. The electrochemical characterization of micro-SOFCs with a 8YSZ bilayer electrolyte and Pt electrodes deposited onto a 500 μm thick Foturan® wafer with an etched hole of 200 μm in diameter yielded an OCV of 0.57 V and a maximum power density of 209 mW/cm^2 at 550 °C. The micro-SOFC performance can be increased in future cells by integrating more stable electrodes and avoiding cracks in the electrochemical membranes.

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