ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

Materials Views
www.MaterialsViews.com

Memristor Kinetics and Diffusion Characteristics for Mixed Anionic-Electronic $SrTiO_{3-\delta}$ Bits: The Memristor-Based Cottrell Analysis Connecting Material to Device Performance

*Felix Messerschmitt, Markus Kubicek, Sebastian Schweiger, and Jennifer L.M. Rupp**

Memristors based on mixed anionic-electronic conducting oxides are promising devices for future data storage and information technology with applications such as non-volatile memory or neuromorphic computing. Unlike transistors solely operating on electronic carriers, these memristors rely, in their switch characteristics, on defect kinetics of both oxygen vacancies and electronic carriers through a valence change mechanism. Here, $Pt|SrTiO_{3-\delta}|Pt$ structures are fabricated as a model material in terms of its mixed defects which show stable resistive switching. To date, experimental proof for memristance is characterized in hysteretic current–voltage profiles; however, the mixed anionic-electronic defect kinetics that can describe the material characteristics in the dynamic resistive switching are still missing. It is shown that chronoamperometry and bias-dependent resistive measurements are powerful methods to gain complimentary insights into material-dependent diffusion characteristics of memristors. For example, capacitive, memristive and limiting currents towards the equilibrium state can successfully be separated. The memristor-based Cottrell analysis is proposed to study diffusion kinetics for mixed conducting memristor materials. It is found that oxygen diffusion coefficients increase up to 3×10^{-15} m^2s^{-1} for applied bias up to 3.8 V for $SrTiO_{3-\delta}$ memristors. These newly accessible diffusion characteristics allow for improving materials and implicate field strength requirements to optimize operation towards enhanced performance metrics for valence change memristors.

1. Introduction

Today's memory technologies, e.g., dynamic random access memory (DRAM) and flash memory, rely heavily on the miniaturization of transistors to maintain the projected performance growth. However the physical limitations of this approach are nearing which emphasizes the need for new technologies to be developed.[1] In recent years, resistive switches deployed as resistive random access memories (ReRAMs), which are a non-volatile type of memory, received extensive interest as a promising candidate for the replacement of current transistor technology. In 2008, Strukov and Williams[2,3] reported a connection to the mathematical memristor concept developed by Chua.[4] In general, a resistive switch can attain different resistance states which are controlled by the polarity or magnitude of an applied bias resulting in pinched hysteretic *I–V* profiles.[5] In recent years, resistive switching has been reported for various classes of materials ranging from sulfides (e.g., Cu_2S, Ag_2S) to binary oxides (e.g., TiO_2, SiO_2, CuO, NiO, CoO, Fe_2O_3, MoO, VO_2) over to complex oxides (e.g., $SrTiO_{3-\delta}$, $(La,Sr)MnO_3$, $(Pr,Ca)MnO_3$, $BaTiO_3$, $(La,Sr)(Co,Fe)O_3$, $CeCu_3Ti_4O_{12}$).[6–9] Among those the most extensively studied switching oxides are already processed in today's semiconductor industry as gate oxides like $SrTiO_{3-\delta}$,[10] SiO_2,[11] $TiO_{2-\delta}$,[12] $Ta_2O_{5-\delta}$[13] or $HfO_{2-\delta}$.[14] For oxide-based memristive systems one has to distinguish between switches whose mechanism relies on mobile metal *cations* and those relying on mobile oxygen *anions*[1]: Electrochemical metallization switches relying on *cations* consist of an active electrode material, e.g., Ag or Cu, from which the cations migrate at high electric fields through an electrolyte forming a metal filament towards a second inactive electrode, e.g., Pt.[15] In contrast, valence change resistive switches rely on oxygen *anion* migration over structural defects (oxygen vacancies) in the oxide under high electric fields. Here, oxygen ionic defects govern the resistive switches' device characteristics relative to the field strength and charge carrier flux history. Although anionic resistive switches are highly promising as novel memory devices their defect kinetics at different electric field strengths and the implication on the memristive device are largely unexamined.

To date, studies on anionic-memristive systems focus primarily on reports of hysteretic and memristive *I–V* profiles of

F. Messerschmitt, Dr. M. Kubicek, S. Schweiger, Prof. J. L. M. Rupp
Electrochemical Materials
ETH Zurich, Hoenggerbergring 64,
8093, Zurich, Switzerland
E-mail: jennifer.rupp@mat.ethz.ch

DOI: 10.1002/adfm.201402286

metal|oxide|metal combinations and their processing. Classically, the memristance of anionic switch devices is only measured by either cyclic voltammetry or the analysis of low and high resistance states addressed by short pulses. Both methods do not directly correlate the oxide's bulk and interface non-equilibrium carrier kinetics or defect thermodynamics to the measurable memristive device performance. Therefore, to establish engineering guidelines for the material selection, the development of new methodology is required to connect the materials' defect kinetics to memristive device performance with respect to switching speed, scalability, endurance, high to low resistance ratio, and power consumption.

Through this work, we focus on strontium titanate, $SrTiO_{3-\delta}$, a well-established mixed conducting memristive oxide to fabricate own memristive cross-bar bit devices. We investigate and apply new methodology to discuss the role of carrier diffusivities on memristive device performance. For this, we introduce the selected oxide material and discuss its defect chemistry and performance with respect to memristors. Additionally, the state-of-the-art methodology in the field for probing memristive devices in view of carrier contributions is carefully examined.

1.1. What is the Role of Defects and Carrier Contributions for Memristive Devices based on $SrTiO_{3-\delta}$?

The perovskite $SrTiO_{3-\delta}$ is a mixed anionic-electronic conducting model material for which classic defect chemistry models are well established and reports of memristive switching devices already exist.

1.1.1. Defect Chemical Consideration

$SrTiO_{3-\delta}$ reveals a simple cubic perovskite structure with intertwined sublattices of TiO_2 and SrO. In this structure, the overlap of the oxygen 2p and cationic Ti 3d-orbitals is rather small with a wide electronic band gap of about E_{Gap} = 3.2 eV.[16,17] As a consequence, the electrical conductivity is rather low for the undoped state and the equilibrium point defect concentrations determine the overall electrical conduction. The defect concentration dependency on temperature, atmosphere, processing or bias can be leveraged. For example, dependent on environmental conditions $SrTiO_{3-\delta}$ exhibits either predominant oxygen ionic conduction via vacancies in the lattice or electronic conduction via holes (p-type) or electrons (n-type) in accordance to its Brouwer diagram, see Rothschild[18] for details. For the targeted application of $SrTiO_{3-\delta}$ as an active oxide component in valence change ReRAMs it has to be noted that these typically operate in air at moderate temperatures, i.e., room temperature up to 80 °C. Extrapolation of typically high temperature derived conductivities and diffusion data studied on bulk undoped $SrTiO_{3-\delta}$ ceramic pellets to these conditions suggest a predominant p-type[19] (hole) conduction mechanism with a low chemical oxygen diffusion coefficient of $\approx 10^{-17}$ m^2s^{-1} in single crystals for ambient conditions.[20] However, it remains unclear whether this hypothesis on the dominating carrier contribution kinetics holds due to the following arguments for memristive devices:

First, extrapolation of high temperature defect models (>500 °C) to room temperature is precarious and one may carefully examine the validity for this rather new room temperature application as memristors. Further review on the high temperature-defect chemistry and conduction models for the material $SrTiO_{3-\delta}$ are given in the excellent studies of Merkle[21] and Waser.[17]

Second, operation of memristive oxides requires high local electric field strength on the oxide film, typically $>10^5$ Vm^{-1}, influencing the defect chemistry and charge transfer characteristics. To date, charge transfer, in terms of the dominant carrier types and according activation energies are predominantly investigated close to 0 V bias and purely discussed with respect to temperature, atmosphere, or microstructure for oxides. This differs to oxide-based memristive devices operating at high electric field strength and ambient conditions.

Third, most models are derived for bulk ceramic pellets and single crystals. The role of thin film-processing related characteristics is rarely discussed for the memristive oxides, i.e., lattice strain, microstrain or simply the grain boundary density may vary and requires debate. In thin films those properties are likely to affect the defect thermodynamics and resulting carrier transport properties or the non-stoichiometry. For example, strain can affect the transport properties changing the local bond strength in doped and undoped $SrTiO_{3-\delta}$ films.[22] Gregori, Maier and co-workers[23–25] discussed the role of space charges for size-effect changes in the grain to grain boundary ratio of thin films. Waser, Guo and co-workers[26] revealed that the Brouwer diagram changes dependent on the variation of space charge volume relative to film thickness and strain state of a $SrTiO_{3-\delta}$ thin film. De Souza highlighted the role of grain boundaries on extended defects in $SrTiO_{3-\delta}$ in theory and experiments.[20,27,28] In addition, amorphous residuals or overall crystalline to amorphous phase content changes can affect the transport kinetics by near order structural changes of such oxide thin films.[29–31] Review contributions of Yildiz[32] and Rupp[33] revealed that lattice strain for thin film processing of oxides can be used as an engineering tool to tune their defect chemistry, transport and non-stoichiometry. Recently, we showed that strain engineering in new types of oxide multilayer micro-dot devices can control anionic conductivity contributions beyond classical doping.[34] Here, first chip-based microcontacting strategies were presented to tune real anionic strain effects for potential moderate temperature applications like resistive switching devices.[34,35]

Therefore, current defect models derived for high temperature bulk pellet ceramics and single crystals need to be carefully tested in their applicability to establish atomistic models for memristive switching in mixed conducting anionic-electronic oxide thin films operated at room-temperature under high electric field strength; as are the prevailing conditions in memristive metal|$SrTiO_{3-\delta}$|metal devices.

1.1.2. Memristive Devices

Several groups demonstrated resistive switching for $SrTiO_{3-\delta}$ with Pt, Ti, Ni, Pd, Au, Nb:$SrTiO_3$ or $SrRuO_3$ electrodes at local electric field strengths of 10^5–10^9 Vm^{-1}.[10,36–41] In these studies

$SrTiO_{3-\delta}$ single crystals or thin films deposited via pulsed laser deposition were examined. A promising endurance of 10^6 cycles, retention of 10^5 s and R_{off}/R_{on} ratio of 100 could be demonstrated for $SrTiO_{3-\delta}$ based memristive switches.[42] The wealth of experience in working with $SrTiO_{3-\delta}$ as a transistor gate oxide on a chip make its integration into future ReRAM devices highly feasible. For further information about integration and specifications of ReRAMs see Refs. [17,43,44]. Different mechanisms for resistive switching and memristance on the atomistic scale were proposed for $SrTiO_{3-\delta}$ in literature and are still under debate: Sawa[45] emphasized the role of the Schottky barrier and of changes along metal|oxide interfaces. Waser and co-workers[37] argue that oxygen vacancy filaments in $SrTiO_{3-\delta}$ are responsible for the resistive switching. Depending on the applied bias amplitude the mechanism could even be changed between filament and homogenous interface type switching on $SrTiO_{3-\delta}$ samples.[10] However, independent of the mechanism the *thermodynamics* of the anionic diffusive species at the high electric fields involved during resistive switching determine the required SET/RESET voltages, read voltages and the range of accessible resistance states for the memristive device. On the other hand, it is the *drift and diffusion kinetics* which define performance specifications of a memristive device such as switching speed and endurance. Therefore, we need new methods to access these fundamental carrier transport parameters for memristive anionic-carrier systems.

1.2. How to Probe Electric Contributions of Charge Carriers and Their Atomistic Role to Memristance?

Today, most electrical measurements in ReRAM research are done either by *pulse experiments* or by *cyclic voltammetry measurements*. Pulse experiments during which the bias pulse is applied for few nano- to micro-seconds are close to later application conditions in computers. Although this method allows directly extracting important specification parameters, it gives only very limited insights into the switching mechanism and in particular into the carrier kinetics.

On the other hand, classic cyclic voltammetry measurements during which the bias is constantly changed with a certain sweep rate are carried out. We can identify in the literature on $SrTiO_{3-\delta}$, that this is the established method to characterize memristive behavior, however, the electric carrier kinetic and thermodynamic parameters involved are not experimentally accessible. This is surprising since their diffusivities and concentrations are the basis of the device characteristics. Several ex situ analyses such as X-ray absorption near edge structure analysis (XANES),[46] X-ray fluorescence,[46] conducting atomic force microscopy (cAFM),[10,47,48] impedance spectroscopy,[47] atom probe microscopy[49] and X-ray photoelectron spectroscopy (XPS)[42] of oxide film microstructures and their defects were reported to reveal the memristive mechanism. Nevertheless, those measurements are rather a snapshot of the defect state and do not allow to develop models depending on the charge carrier flux. Computational work by the groups of Riess[50–52] and Strukov[53] have successfully demonstrated that the shape, magnitude, and number of resistance states in memristive I–V profiles can be related to carrier diffusivities and flux for mixed conducting oxides.

It is important to note that very recently the experimental methodology to connect carrier transport kinetics to memristance was extended for *cationic-switches* by Waser and coworkers.[15] The authors described the switching kinetics from cyclic voltammetry measurements by applying the Randles-Sevcik[54] equation for a $Pt|Cu|SiO_2|Pt$ device operating on Cu-filament formation. However, in mixed anionic-electronic memristive oxide systems, such as for the $SrTiO_{3-\delta}$ system, the dominant electronic carriers always superpose the anionic currents of the switching species, making the system inapplicable for Randles-Sevcik analysis[55] (ionic transference number << 1). The major challenge is to identify additional methodology to probe the carrier kinetics that drive the anionic resistive switching devices beyond the classic methods of pulse experiments and cyclic voltammetry. Direct comparison of these parameters allows studying materials compositions and tuning of material constituents to fit the purpose and to establish engineering guidelines for material selection for memristor devices.

To this end, we develop 2-terminal $Pt|SrTiO_{3-\delta}|Pt$ based multi-bit memristive cross-bar device structures. These can be used to systematically investigate resistive switching characteristics and kinetics for a model mixed anionic-electronic conducting oxide. In standard memristive device tests of mixed electronic-anionic conducting oxides it is difficult if not impossible to distinguish between the dominant charge carrier type and its diffusion kinetics with respect to the device's field strength and bias history. We discuss the potential and limitations in terms of carrier kinetic evaluation for classic cyclic voltammetry of mixed conducting, $SrTiO_{3-\delta}$, memristive bits and extend the classic electrochemical methods by two new approaches being bias-dependent activation energy measurements and chronoamperometry for memristors. Through this new methodology, dominant carrier types, time constants and diffusion coefficients can be determined with respect to applied bias as driving force for the memristive devices: First, we investigate the dependency of the electrical conductivity activation energy on high electric fields and polarity of bias, to get a more complete picture of the dominating carrier transport mechanism involved in resistive switching. Second, we develop the analysis method for chronoamperometry measurements for mixed conducting memristive oxide devices to study the defect kinetics and thermodynamics as transients to bias applied. Here, we demonstrate that three regimes can be ascribed being dominated either by a capacitive-like or memristive current or a limiting current close to thermodynamic defect equilibrium with respect to bias and polarity operated. This work presents the first description of a memristor-based Cottrell equation and gives the basis for analysis of material-dependent carrier diffusion coefficients in mixed conducting anionic-electronic memristors. Through smart choice of mixed conducting oxide materials based on now accessible kinetic characteristics under bias one can directly influence future electric circuit device designs and tune the memristive bit operation in terms of their time constants, threshold voltage for switching and equilibrated resistance states, for example tune their low to high resistance state ratio, read/write voltages, power consumption and endurance.

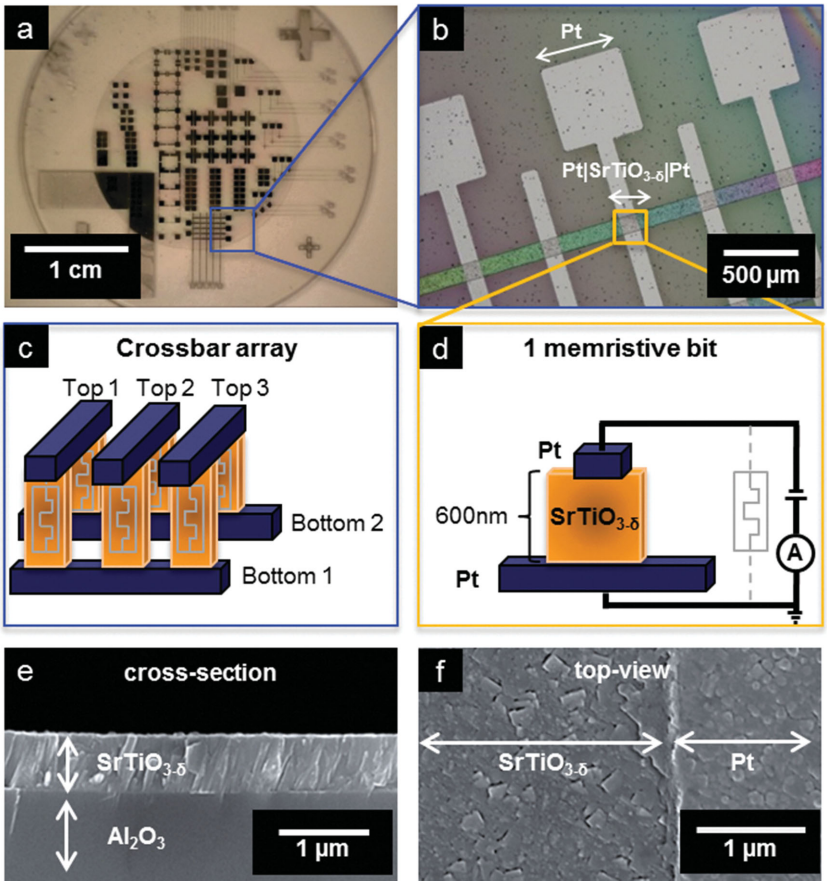

Figure 1. a) Photograph of a multi bit Pt|$SrTiO_{3-\delta}$|Pt memristive device structure with in- and cross-plane 2-terminal electrode geometries. b) High magnification image of cross-bar array showing 5 memristive Pt|$SrTiO_{3-\delta}$|Pt bits. c) Schematic cross plane view of addressable multi-bit memristor structures for cross-bar array and for d) single bit with equivalent circuit symbol. e) SEM cross-sectional image showing dense columnar polycrystalline growth of oxide $SrTiO_{3-\delta}$ film via PLD with 620 nm in thickness. f) SEM top-view image of platinum electrode and $SrTiO_{3-\delta}$ film.

2. Results and Discussion

2.1. Two-Terminal Pt|$SrTiO_{3-\delta}$|Pt Memristive Device Fabrication for an Addressable Cross-Bar Array

For the experiments, we microfabricated Pt|$SrTiO_{3-\delta}$|Pt memristive elements in a cross-bar array electrode structure. A photograph of a prepared sample with up to 25 addressable memristive Pt|$SrTiO_{3-\delta}$|Pt "bits" is shown in **Figure 1**a. Here, different 2-terminal micro electrode geometries are demonstrated that were processed for in-plane and cross-plane electrical measurements of single Pt|$SrTiO_{3-\delta}$|Pt bits down to a feature size of 25 µm. The $SrTiO_{3-\delta}$ metal oxide components of the memristive device structures were fabricated by pulsed laser deposition (PLD) with a targeted film thickness of 600 nm and Pt electrodes via electron beam physical vapor deposition (EBPVD) with 80–150 nm in thickness. A light microscopy image and magnification of a cross-bar array device structure of 25 separately addressable bits are shown in Figure 1b. The cross-bar array suited as a possible high packaging density circuit design for 2-terminal ReRAMs[56,57] is schematically shown in Figure 1c. One bit consists of two platinum electrodes and a $SrTiO_{3-\delta}$ thin film in-between as active anionic-switching material for a cross-plane configuration as shown in Figure 1d. X-ray diffraction (XRD) confirms the cubic $SrTiO_{3-\delta}$ phase for the metal oxides in the memristive bits in accordance with Abramov et al.,[58] see Supporting Information Figure S1. The cross-plane scanning electron microscope (SEM) image displays a dense microstructure and typical columnar grain growth for the $SrTiO_{3-\delta}$ thin film elements of targeted thickness (also confirmed by profilometer), Figure 1e-f. This is in agreement with earlier studies on PLD growth of perovskite thin films.[22,59]

2.2. Measuring Memristance of Pt|$SrTiO_{3-\delta}$|Pt bits in a Cross-Bar Array Device via Classic Cyclic Voltammetry

The current–voltage (*I–V*) profile of a single Pt|$SrTiO_{3-\delta}$|Pt bit element addressed in a cross-bar array is shown for 30 consecutive cyclic voltammetry measurements in **Figure 2**a. A hysteretic *I–V* characteristic is observed depending on the applied SET and RESET voltages and current direction (polarity) for the memristive bit element at a constant sweep rate of 50 mVs^{-1}. Applying an increasing positive bias up to a SET voltage of +4 V to the top electrode of the structure strongly increases the current and switches the bit from its high resistance state, *HRS*, (OFF state) to its low resistance state, *LRS*, (ON state). Reversing the polarity of the bias switches the resistance state back from low (ON) to high (OFF) at a RESET voltage of –4 V for a bit. Based on the analyzed hysteretic *I–V* profiles, a bipolar memristive characteristic can be assigned for the single Pt|$SrTiO_{3-\delta}$|Pt bits which is in accordance to earlier reports of Menzel et al.[37] and Janousch et al.[46] viz. a non-volatile memristive behavior is confirmed by the pinched hysteretic profile. A bias of ±4 V and the corresponding switching current are clearly low enough to prevent the bit from unipolar switching as reported by Menzel et al.[37] We calculated the electric field strength at switching as 6.5×10^6 Vm^{-1}, which is comparable to that of thin film devices based on $SrTiO_{3-\delta}$ in the field.[10,36–41] The switching endurance was confirmed for more than 200 consecutive cycles in the cyclic voltammetry measurements, see Supporting Information Figure S2. It is worth mentioning that the stable resistance states of a $SrTiO_{3-\delta}$ switch depend not only on the history but also on the atmosphere, especially the humidity; similar dependencies were also recently reported for cation-based switches.[60]

Bipolar memristive switching $SrTiO_{3-\delta}$ oxide elements rely on a redox-valence change mechanism altering electrical carrier contribution via defect movement upon bias and current flux history. We analyzed the time-dependence

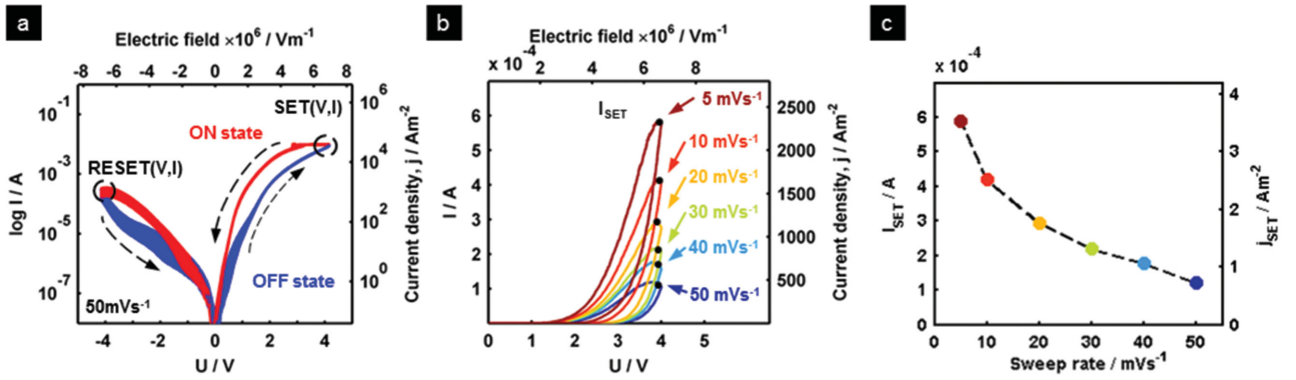

Figure 2. Memristive Pt|$SrTiO_{3-\delta}$|Pt bit characterized via cyclic voltammetry: a) *I–V* profiles showing stable hysteretic bipolar memristive switching characteristic at a constant sweep rate of 50 mVs^{-1} for 30 consecutive cycles. b) *I–V* profiles for systematically decreased sweep rates to probe the time-dependence of the memristance. c) Plot of SET current, I_{SET}, against sweep rate illustrating the different resistive states that are accessible with respect to sweep rate. The electric field strength and current density are indicated in the plots a)-b) and set current density, j_{SET} in the plot c).

of the memristance by variation of the sweep rate for fixed SET and RESET voltages of ±4 V for a single Pt|$SrTiO_{3-\delta}$|Pt bit, Figure 2b. The SET current, I_{SET}, defining the ON resistance state systematically increases by a factor of 4.8 when decreasing the sweep rate by one order of magnitude from 50 to 5 mVs^{-1} (+4 V). As expected, the ON resistance drops from 33.1 MΩ (13.3 MΩm) to 7.8 MΩ (3.1 MΩm) and the memristive hysteretic *I–V* loop is enlarged; viz. the involved local charge carrier concentration profiles are in a metastable time-dependent state for similar electric field strength. We summarize the decreasing SET current and the respective current density for the increase in sweep rate in Figure 2c. Comparison to literature reveals that this time dependent behavior is typical for resistive switching and reflects the metastable defect state of the memristive Pt|$SrTiO_{3-\delta}$|Pt bits presented.[61] To attain a precise kinetically equilibrated resistance state, even lower sweep rates than 5 mVs^{-1} would be required for $SrTiO_{3-\delta}$-based switches. This is in accordance with simulations on perovskite memristive switches[37] and experiments on $SrTiO_{3-\delta}$ and Cr:$SrZrO_3$.[37,62]

We conclude from these findings that this anionic-electronic conducting memristive system remains in a metastable state during cyclic voltammetry measurements. Obviously, at significantly shorter times as commonly used in pulsed experiments such a stable state cannot be reached either. With these standard methods it is challenging if not impossible to come to a conclusion on the underlying resistive switching mechanism and defect kinetics for a memristive anionic-electronic bit. However, in order to predict the materials switching behavior on writing and erasing bias pulses in ReRAMs and voltage-to-time operation schemes it is highly important to define the kinetics of involved carrier processes. In the following, we therefore suggest two new methodology approaches based on bias-dependent activation energy measurements and chronoamperometry to investigate the anionic and electronic defects and their charge carrier diffusivities as complimentary tools in the memristor field. We discuss the involved defects and carriers with respect to the programming voltage (SET), field strength, and operation parameters to determine their impact on memristance of Pt|$SrTiO_{3-\delta}$|Pt bits.

2.3. Bias-Dependent Carrier Kinetics and Their Activation Energies in Memristive Pt|$SrTiO_{3-\delta}$|Pt bits

We investigated the electric conductivity and their activation energies for single Pt|$SrTiO_{3-\delta}$|Pt bits for a rather unusual wide bias range of 0.1 V to 3 V with respect to carrier flux direction (polarity), **Figure 3**. This corresponds to an electric field strength of up to 5×10^6 Vm^{-1} for the given device geometry. The effect of an external bias stimulus on a memristive Pt|$SrTiO_{3-\delta}$|Pt bit can alter both its *metal-oxide interfacial* and *bulk oxide* transport, see schematic Figure 3a: For instance, by applying an electric field the Schottky barrier height at the *metal-oxide interfaces* and their metal-oxide band bending can be altered. On the other hand the *oxide* can exchange oxygen in a reaction with the gas phase whereby its oxide non-stoichiometry can be modified. In the following, we examine the Arrhenius-type dependence of electric conductivity with respect to the applied bias and polarity for a Pt|$SrTiO_{3-\delta}$|Pt bit, Figure 3b-d:

First, we measure the temperature dependence of conductivity by applying a small bias of +0.1 V, Figure 3b: The activation energy of conductivity was calculated as equal to 1.40 ± 0.07 eV. This is in good agreement with literature data of pellets for $SrTiO_{3-\delta}$ for which 1.45 eV[23] and 1.52 eV[63] were reported for similar small bias and temperatures. The authors further confirmed by impedance spectroscopy analysis that electronic conduction along grain boundaries is predominant.[23,63] In accordance, it is reasonable to ascribe a *predominant p-type conduction* mechanism for the memristive bits tested at 0.1 V bias stimulus in air in this study.

Second, for positive bias (top-electrode positive) up to 3 V, Figure 3b: A clear drop in activation energy by Δ0.24 eV to 1.16 ± 0.07 eV is measurable for increasing bias strength from 0.1 to 3 V. In consistency, the overall conductivity is also observed to increase for larger bias.

Third, for negative bias (top-electrode negative) up to –3 V, Figure 3c: Switching the polarity to negative bias reduces similarly the activation energy to 1.24 ± 0.16 eV for –3 V. All measured electrodes on both samples show a similar temperature-dependent electrical conductivity independent on the heating and cooling cycle. Therefore, it can be concluded that all fabricated switches have comparable chemistry and a

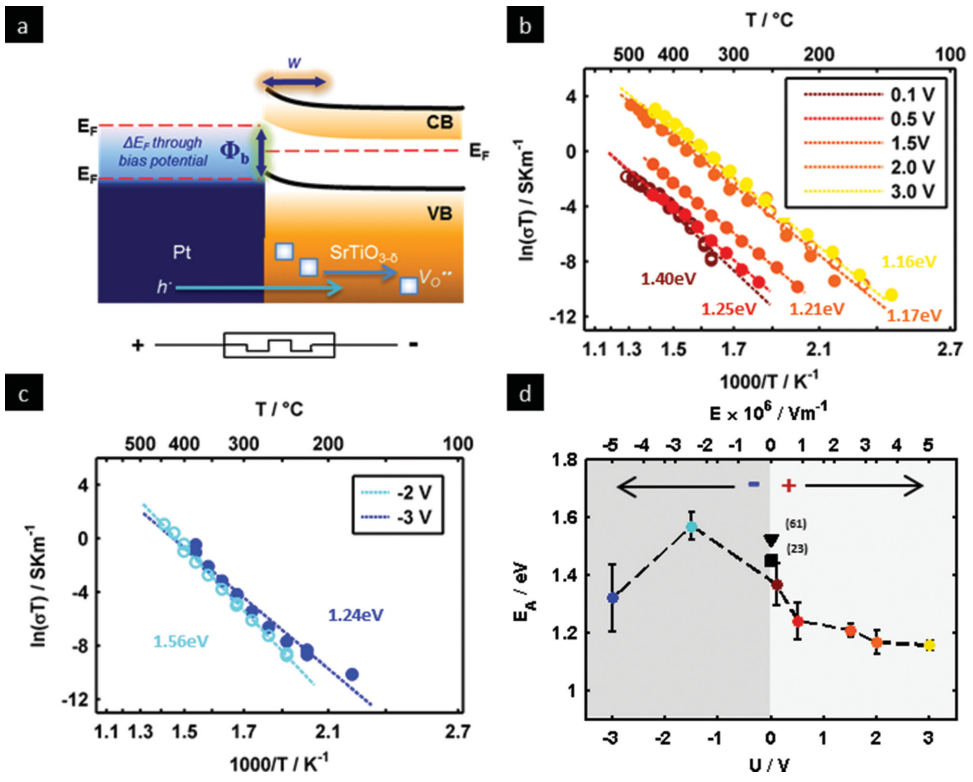

Figure 3. a) Schematic showing the bias-dependent Schottky barrier height of one single interface and the alteration of the oxygen vacancy depletion zone for a Pt|$SrTiO_{3-\delta}$|Pt memristor bit. b) Arrhenius plot of electric conductivity for positive bias (top electrode) during heating (open symbols) and cooling (filled symbols). c) Arrhenius plot of electric conductivity for negative bias (top electrode). d) Calculated activation energies with respect to bias as driving force for a Pt|$SrTiO_{3-\delta}$|Pt memristor bit including reference data from literature for 0.1 V.[23,61]

good adhesion of the platinum electrodes before, during and after electric testing under bias and temperature. To the best of our knowledge these bias-dependent activation energy conduction measurements are new to the field and can consequently not be compared to literature of anionic-oxide based memristors.

We observe that both, the increase of positive as well as negative bias, lower the activation energy. The following changes in ionic or electronic defects under bias may account for the experimental finding: i) the Schottky barrier height (Φ_b) at one *metal|oxide interface* is systematically lowered. ii) The concentrations and mobilities of the vacancy defects are increased under bias. Comparing with values from literature for a p-type electronic conduction along grain boundaries, we would expect an activation energy of 1.5 eV and for the *oxide bulk* an activation energy of ~1 eV.[24] Therefore, a pronounced conduction of the bulk could be possible at higher electric fields. iii) Joule heating within the *oxide bulk* might take place and has to be taken into account responsible for an increased conductivity at lower temperatures for higher electric fields as shown in simulations resulting in a falsely too low activation energy.[37] We can exclude Joule heating as dominant factor in our experiments as we will show later in the discussion of the diffusion coefficients.

Interestingly, we observe an overall asymmetry in the decay of the activation energy for increasing bias magnitude with respect to the applied polarity to the device, see Figure 3d. We further report bipolar current–voltages profiles, which are asymmetric with respect to polarity in the cyclic voltammetry characteristics, Figure 2a. Taking both experimental evidences into account, this essential asymmetry for bipolar resistive switching exists despite the symmetric Pt|$SrTiO_{3-\delta}$|Pt electrode-oxide design and methodology applied. On the one hand, variations in the oxygen surface adsorption reaction may exist, since the Pt electrodes and their exposure to air is not symmetric. The top electrode is exposed with the whole surface to air and the oxide, and the bottom electrode is located between the substrate and oxide, Figure 1e. On the other hand, a different PLD film growth close to and further away from the substrate may result in an asymmetric thin film microstructure.[64] Another possible origin of the observed asymmetry could also be caused by the first cycle in a pristine bit depending on the bias polarity applied first to the electrodes similar as described in literature for electroforming, see Rodenbucher et al.[49] We can clearly exclude the electroforming to account for the asymmetry in presented Pt|$SrTiO_{3-\delta}$|Pt bits as the same hysteresis direction was observed independent on the firstly applied bias direction (polarity). Therefore, we conclude that either the variations in oxygen surface adsorption of the electrode-gas interface or the anisotropy of typical PLD-processed thin film microstructures may be accounted for the observed asymmetry in the bias-dependent activation energies for the Pt|$SrTiO_{3-\delta}$|Pt bit conductivities.

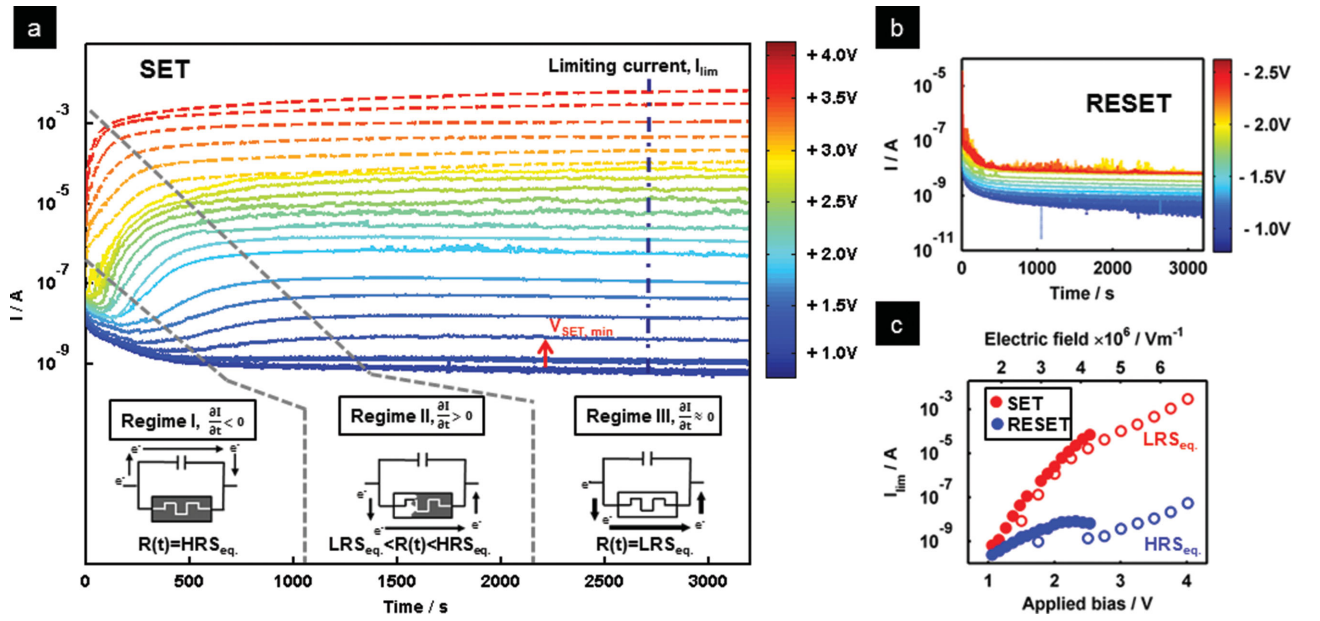

Figure 4. Results of chronoamperometry experiments measured on different bits for increasing bias voltage (solid lines and symbols) and decreasing bias voltage (dashed lines, open symbols): a) Evolvement of current over time with respect to constant bias measured for a Pt|$SrTiO_{3-\delta}$|Pt-bit structure via chronoamperometry. For a SET bias range three regimes can be identified: I. Decay of current with respect to time indicating the *capacitive regime*. II. Increasing conductivity is measured with respect to time for a specific minimum SET threshold voltage of $V_{SET, min}$ = 1.2 V indicating the memristive nature and switching of the device. III. Stable *limting current*, I_{lim}, is reached. The circuit elements are indicated in accordance to the regime. b) Exemplary chronoamperometry data for a RESET bias range of –1.0 V to –2.5 V until an equilibrated high resistance state is reached, $HRS_{eq.}$. c) Equilibrated high and low resistance states ($HRS_{eq.}$ and $LRS_{eq.}$) with respect to applied bias showing the accessible resistance states for a given bias.

2.4. Chronoamperometry to Investigate Material-Dependent Diffusion Characteristics for Memristive Pt|$SrTiO_{3-\delta}$|Pt Bits

In the following, we investigate the method of chronoamperometry to probe anionic diffusion contributions for memristive Pt|$SrTiO_{3-\delta}$|Pt bits. In this method, the current evolution is followed over time with respect to a constant applied bias. Classic examples of the method can be studied in the battery field for details see e.g., Bard et al.[55] We newly apply and test the method for memristive bits whereby well-defined equilibrium states can be studied in contrast to classic cyclic voltammetry experiments.

Figure 4 displays the chronoamperometry characteristics of a Pt|$SrTiO_{3-\delta}$|Pt bit in the cross-bar array structure for which the current evolution over time is studied for constant bias in the range of 1.0 to 4.0 V. Figure 4a shows the chronoamperometry characteristics for a positive constant bias applied to the top electrode (SET voltage) for 2 hours. Between every bias step the according negative bias (RESET voltage) is applied for at least an hour to completely reset the device and set it into its equilibrated OFF state again, see Figure 4b. The time interval is chosen so that the electric current is measured until a stable equilibrated limiting current, I_{lim}, is reached, Figure 4c. The reproducibility of the data is proven by two independent Pt|$SrTiO_{3-\delta}$|Pt bits, where the SET/RESET voltage is increased in Δ0.1 V steps (full lines & solid symbols) and decreased on a different bit (dashed lines & open symbols). Therefore, we can conclude the current evolution over time is independent of the bias step direction and the SET/RESET process is fully reversible. Although the method of chronoamperometry was already used on similar perovskite oxides in the 1960s and 70s,[65,66] the time and bias dependency of the current was so far neither discussed in detail nor put into relation for application and description of memristors. We exemplify on the SET states of a Pt|$SrTiO_{3-\delta}$|Pt bit that the current over time characteristics at constant bias can be categorized into three regimes, denoted as I-III in Figure 4a:

Regime I $\left(\frac{dI}{dt} < 0\right)$: The current drops during the first seconds for a constant bias stimulus applied. This current drop points strongly towards capacitive processes being responsible for dI/dt < 0 as denoted in the circuit model of Figure 4a, although a slightly flatter and no purely exponential decay of the current is observed. This regime gets less pronounced at higher voltages until it vanishes completely for SET voltages >2.8 V.

Regime II $\left(\frac{dI}{dt} > 0\right)$: In this regime the current increases over time until a stable limiting current is reached. For an applied bias range <1.2 V, however, this regime is not visible. This means that the voltage as external stimulus is too low to activate the processes responsible for memristive behavior resulting in increased conductivity. Thus, at low bias voltages the resistive portion stays unchanged in its high resistance state, $R(t) = HRS_{eq.}$(OFF), see Figure 3a. Only the capacitive current decay of regime I is visible until a stable current is reached as depicted in the circuit model analogy for regime I. At a critical threshold voltage of 1.2 V, however, the memristive mechanism gets activated at the external stimulus of bias and regime II is observable. This threshold voltage defines the minimum SET Voltage, $V_{SET,min}$, of our Pt|$SrTiO_{3-\delta}$|Pt device. The device switches from its equilibrated

high resistance state, $HRS_{eq.}$ (OFF), to its equilibrated low resistance state, $LRS_{eq.}$ (ON), as depicted in the equivalent circuit diagram for regime II, $LRS_{eq.} < R(t) < HRS_{eq.}$. From today's common understanding of oxygen vacancy migration as responsible resistive switching mechanism in anionic memristive devices,[17] we conclude oxygen vacancy motion lowers the overall electronic resistance of the device in regime II. It has to be mentioned that this critical threshold voltage of the resistive switching mechanism is not accessible via cycling voltammetry experiments, but defines a fundamental new material parameter for resistive switching devices. Especially for the discussion and improvement of required switching voltages and non-volatility in final devices this material characteristic threshold voltage might be crucial. Increasing the bias magnitude reduces the time interval of regime II. A detailed discussion of the time characteristics and diffusion coefficients of the processes will form the basis of the subsequent chapter.

Regime III $\left(\frac{dI}{dt} \approx 0\right)$: In the final state dI/dt equals zero and a stable limiting current, I_{lim}, prevails, as quantified in relation to the field strength in Figure 4c. The device reaches an equilibrated state at which the electronic conduction is constant, R(t) = $LRS_{eq.}$. Therefore, assuming a redistribution of oxygen vacancies as cause for the increase of the conductivity in regime II we can also conclude that this redistribution has reached a final state by a drift-diffusion equilibrium of oxygen vacancies at the according bias in regime III. The resistance in this equilibrium state defines the limiting lowest accessible resistance state, $LRS_{eq.}$, in cycling voltammetry and pulsed experiments for a SET operation in relation to the corresponding bias and electric field strength for the materials involved and device geometry. We analyze an exponential dependency of the limiting current on field strength and bias applied for the low resistance state (ON), see Figure 4c. For common sweep rates in cycling voltammetry experiments usually a non-equilibrated resistance value between $LRS_{eq.}$ and $HRS_{eq.}$ is measured depending on the field strength and charge carrier flux history. This characteristic data is especially interesting to compare material combinations and processing to improve the ON/OFF ratio of resistive switches and to study accessible multilevel switching states for a certain device.

2.5. Bias-Dependent Kinetic Analysis of Carrier Diffusion for a Memristive Pt|$SrTiO_{3-\delta}$|Pt bit via Chronoamperometry Measurements: The Memristor-Based Cottrell Analysis

On the basis of the suggested circuit model of a parallel memristor-capacitor to represent the Pt|$SrTiO_{3-\delta}$|Pt bit, we will determine the time constant, τ, of regime II, $\left(\frac{dI}{dt} > 0\right)$ relative to bias for kinetic analysis of diffusing carriers in the following.

For the analysis of diffusion kinetics in chronoamperometry experiments classically the Cottrell equation (Equation (1)) is applied which describes the change in diffusion-controlled current response with respect to a constant potential:

$$i_j = \frac{nFAc_j^0\sqrt{D_j}}{\sqrt{\pi t}} \quad (1)$$

where i_j represents the diffusion current, n the number of electrons transferred, F the Faraday constant, A the geometric electrode area, t the time, c_j^0 the bulk concentration of the diffusive species and D_j the chemical diffusion coefficient. In a classic electrochemical system (e.g., a redox couple in a battery) one measures a diffusion current resulting in a current drop to zero for time approaching infinity with $i_j \propto t^{-0.5}$ in accordance to Fick's law.[55] In contrast to the classic behavior, the chronoamperometry results for our memristive Pt|$SrTiO_{3-\delta}$|Pt device reveal for the regime II in Figure 4a an increasing current over time indicating the memristive nature and switching of high to low resistance state upon bias which makes an adaption of the Cottrell equation necessary.

The total electric current, i_{total}, can be described by the sum of the electronic, $i_{e'}$ and $i_{h^\cdot}$, and oxygen ionic currents, $i_{V_O^{\cdot\cdot}}$, of $SrTiO_{3-\delta}$, namely,

$$i_{total} = i_{e'} + i_{h^\cdot} + i_{V_O^{\cdot\cdot}} \quad (2)$$

In particular, the electric conductivity is dictated by the mobility, η_j, and concentration, c_j, of the single charge carrier species, j, and the elementary charge, q:

$$i_{total} = q\eta_{h^\cdot}c_{h^\cdot} - q\eta_{e'}c_{e'} + 2q\eta_{V_O^{\cdot\cdot}}c_{V_O^{\cdot\cdot}} \quad (3)$$

The total concentration of oxygen vacancies, $c_{V_O^{\cdot\cdot}}$, in $SrTiO_{3-\delta}$ can be described according to the oxygen exchange reaction:

$$V_O^{\cdot\cdot} + \frac{1}{2}O_2(g) \rightleftharpoons O_O^x + 2h^\cdot \quad (4)$$

Here, the Kröger-Vink notation is used and (g) is referred to the gas phase.

Based on the careful analysis of the bias-dependent activation energy of transport in the Pt|$SrTiO_{3-\delta}$|Pt bits we account electronic carriers, namely p-type, to be predominant. Although the current is mainly carried by electronic carriers, we suggest in accordance with today's common understanding oxygen vacancy drift and diffusion as responsible switching mechanism in anionic-electronic devices. Therefore, we account for the memristive nature in regime II by a modification of the Cottrell equation to describe the time constant characteristic relative to bias, see **Figure 5**a-d. For a memristive system the increase in current over time till a limiting current is reached (e.g., region II, Figure 4a) can be defined by a differential current, I_d:

$$I_d(t) = I_{lim} - I(t) \quad (5)$$

We can now rearrange the classic Cottrell equation, Equation (1), use the differential transient memristor current data to evaluate the diffusion coefficient, D_m, by defining a memristor-based Cottrell equation accounting for the valence change mechanism:

$$D_m = \left(\frac{\left(I_d\sqrt{t}\right)\sqrt{\pi}}{nFA\Delta c}\right)^2 \quad (6)$$

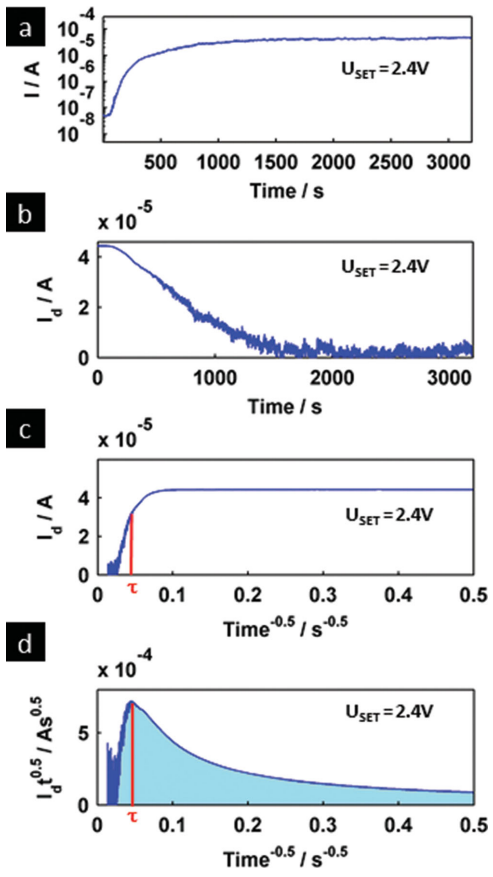

Figure 5. Example of kinetic analysis steps to calculate with the memristor-based Cottrell equation the material specific time constant, τ, for the memristive regime II for a constant applied bias on Pt|$SrTiO_{3-\delta}$|Pt bits: a) Measurement data of chronoamperometry experiment for an applied bias of +2.4 V to the top electrode in logarithmic scale. b) Differential current, I_d, allowing to analyze the oxygen diffusion. c) The plotted $I_d(t)$ vs $t^{-0.5}$ curve. d) The $I_d(t)\ t^{0.5}$ vs $t^{-0.5}$ curve to derive the material specific time constant, τ, for the memristive regime II.

Here, the time, τ, is a material-dependent time constant and is defined as at which $I\sqrt{t}$ has its maximum with respect to bias given by:

$$t(\tau) := \left\langle \left[I_{\lim} - I(t) \right] \sqrt{t} \right\rangle_{\max} \tag{7}$$

This maximum approach is typically used in literature to extract diffusion constants from chronoamperometry experiments.[67] On the basis of Equations (5) to (7), the time constant can be analyzed with respect to bias for the valence-change memristor bit. In Figure 5a-d, we exemplify the analysis for a set bias of +2.4 V and extract a time constant of 291 s. The time constants are displayed for the measured bias range of 1.2 V to 3.9 V in **Figure 6**a. A decrease in time constants of about a factor seven (876 to 129 s) is measured for an increase in bias up to +3.9 V for a Pt|$SrTiO_{3-\delta}$|Pt bit. Assuming that the whole oxide volume between the electrodes contributes to the memristive current increase under bias, the diffusion coefficient is evaluated using the time constants derived in Equation (6) and (7) according to the memristor-based Cottrell equation, see Figure 6b. We base our calculation on an experimentally determined diffusion length of 620 nm electrode distance by SEM and profilometry for one Pt|$SrTiO_{3-\delta}$|Pt bit. We observe a maximum in diffusion coefficient of 3×10^{-15} m^2s^{-1} at 3.8 V bias which reduces to 4×10^{-16} m^2s^{-1} for 1.2 V bias at room temperature. This dependency reveals how strong the oxygen migration is facilitated by the electric field. Literature comparison to chemical oxygen vacancy diffusion data of $SrTiO_3$ single crystals for high temperature without bias as driving force were extrapolated to ambient conditions[20,68–70] and result in diffusion coefficients in the range of 6×10^{-17} m^2s^{-1} – 4×10^{-19} m^2s^{-1}, Figure 6b. Interestingly, this reveals that the diffusion coefficients derived in this study for the memristive bits are of comparable magnitude and in agreement with De Souza's global expression of diffusion coefficient for room temperature and zero bias extrapolation.[20] This implies that indeed oxygen vacancy diffusion is responsible for the resist-

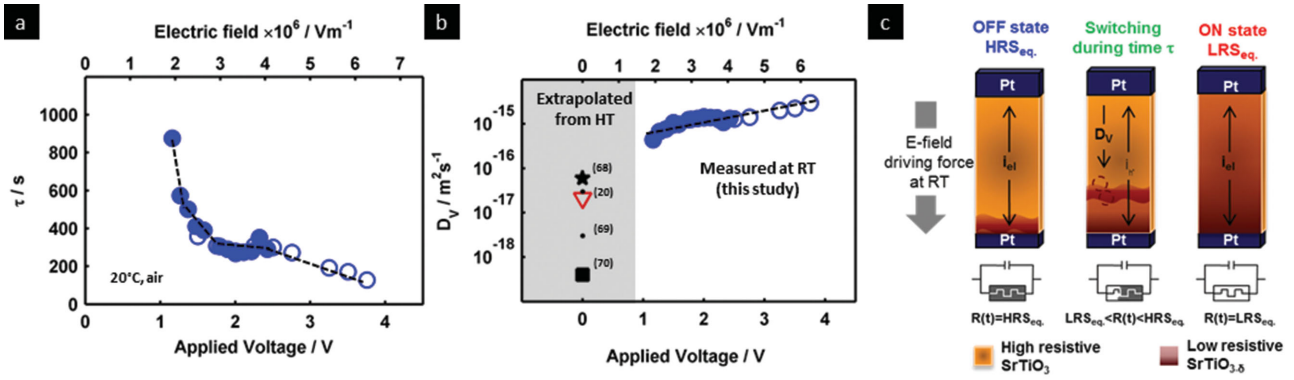

Figure 6. Analysis of specific time and diffusion constants for a memristive Pt|$SrTiO_{3-\delta}$|Pt bit via the memristor-based Cottrell equation: a) Analyzed time constant, τ, determined via the memristor-based Cottrell equation for the memristive oxide $SrTiO_{3-\delta}$ with respect to electric field strength and bias at room temperature for increasing bias voltage (solid symbols) and decreasing bias voltage (open symbols). b) Calculated oxygen vacancy diffusion constant, D_V, for the memristive oxide $SrTiO_{3-\delta}$ with respect to electric field strength and bias at room temperature. Extrapolation of literature vacancy diffusion constants to room temperature without electric field, see Refs. [20,68–70] including De Souza's[20] derived global expression (red triangle) is added for comparison. c) Schematic of resistive switching in $SrTiO_{3-\delta}$ caused by oxygen vacancy redistribution under high electric field at room temperature. In the OFF state the memristive oxide remains unchanged in its high resistance state. At a specific threshold voltage the oxygen vacancies start to redistribute within the oxide decreasing the resistance. In the equilibrated low resistance state the redistribution has reached a final state by a drift-diffusion equilibrium of oxygen vacancies at the according bias.

ance changes in the memristive regime for the Pt|$SrTiO_{3-\delta}$|Pt bits. Here, local changes in oxygen non-stoichiometry of the oxide result and are balanced with electronic carriers at high electric field strength, as depicted in the schematic of Figure 6c.

The extrapolation of diffusion data additionally shows, that an increase of an order of magnitude of the diffusion coefficient equals about ~30 °C increase in temperature. Therefore, we exclude Joule heating as responsible memristive switching mechanism for the given materials and bit structure as larger differences would have been observed within the investigated bias range.

It is promising that based on the memristor-based Cottrell equation diffusion coefficients can be analyzed over the whole range of bias and electric field based on chronoamperometry measurements. These are complementary and give important new material characteristics for mixed anionic-electronic conducting oxides for memristive devices. Additionally, the threshold electric field strength initiating the switch from a capacitive to a memristive behavior can clearly be defined from the transients on the example of the Pt|$SrTiO_{3-\delta}$|Pt bit (i.e., 1.9×10^6 Vm^{-1}) towards the equilibrium limiting currents of the devices. For classic memristor characterization, e.g., cyclic voltammetry, the equilibration and limiting currents remain unknown. Through the new approach demonstrated we can clearly define the diffusion coefficient, minimum field strength and limiting currents for the memristive regime of a Pt|$SrTiO_{3-\delta}$|Pt bit. These are important material characteristics that directly implicate the device design and optimized operation of mixed anionic-electronic oxide-based memristors vs. carrier flux.

3. Conclusion

In this work, we demonstrate that chronoamperometry and bias-dependent activation energy measurements are powerful methods for gaining complimentary insights on material-dependent carrier characteristics for mixed anionic-electronic conducting oxides in memristive devices. Successfully fabricated 2-terminal Pt|$SrTiO_{3-\delta}$|Pt based multi-bit cross-bar structures enable us to define the model oxide constituents in terms of their mixed defects and to investigate the effect of electric field strength and carrier flux on devices memristance. Our results for the Pt|$SrTiO_{3-\delta}$|Pt bits show reproducible and stable resistive switching for state-of-the art cycling voltammetry measurements on several Pt|$SrTiO_{3-\delta}$|Pt bits for $V_{SET,RESET} = \pm 4$ V at field strength of 6.5×10^6 Vm^{-1}. To date, memristor-based kinetic analysis of carriers is focused primarily on one type of defect (cationic) and analyzed via the Randles-Sevcik equation of cyclic voltammetry only. By careful analysis and discussion we highlight the limitations of this classic methodology in characterizing memristance for mixed anionic-electronic oxide-based memristor bits; e.g., it is impossible to determine material-dependent limiting currents, equilibrium defect states, or diffusion characteristics as the involved anionic vs. electronic carrier contributions cannot be separated. This accounts for the development of a comprehensive theory on carrier contribution and kinetics in memristive devices based on oxides with mixed anionic-electronic transport. We overcome these limitations by the use of a combination of complementary methods to identify the oxide material-dependent dominant carrier defect types contributing to the low and high resistance states, and to extract diffusion coefficients with respect to the local electric field strength and write/read voltages of the memristive bits:

First, we investigated the temperature dependence of electric conductivity and calculated activation energies for a rather unusually wide bias range. These measurements revealed a severe decay of activation energy from 1.4 eV down to 1.16 eV for higher biases and an asymmetry with respect to bias polarization as the Schottky barrier is lowered. Based on the activation energies, a predominant p-type electronic conduction balanced by oxygen vacancies of the oxide is a reasonable model to account for the resistive switching in the Pt|$SrTiO_{3-\delta}$|Pt bits in air.

Second, we introduce chronoamperometry to identify the electric field dependence of the capacitive to memristive regimes of the device. Here we applied constant SET and RESET biases to the device during which the memristor bits equilibrate at either low or high resistance states. Oxide-material characteristic time-constants could be measured for which the memristive current evolution dominates in the device with respect to field strength. For example a specific threshold voltage of 1.2 V corresponding to an electric field strength of 1.9×10^6 Vm^{-1} is found for $SrTiO_{3-\delta}$ thin films at which the resistive switching mechanism gets thermodynamically activated at room temperature. Correlating the limiting current to the electric field strength the mixed oxygen anionic-electronic diffusion kinetics were probed via the newly suggested memristor-based Cottrell equation. We found faster diffusion kinetics at higher electric fields with diffusion coefficients ranging from 4×10^{-16} m^2s^{-1} to 3×10^{-15} m^2s^{-1} for a bias increase from 1.2 V to 3.8 V respectively. Comparison to De Souza's global expression of diffusion coefficients for $SrTiO_3$ resulting in 2×10^{-17} m^2s^{-1} reveals a good agreement.[20]

To date, memristor-based kinetic analysis of carriers is focused primarily on *one type* of defect (cationic) and analyzed via the Randles-Sevcik equation from cyclic voltammetry only. We demonstrate an extended strategy to analyze memristive oxide devices kinetics for *two types* of charge carriers, namely, anionic and electronic carriers based on the memristor-based Cottrell analysis and the method of chronoamperometry. Here, classic kinetic analysis via the Randles-Sevcik equation would no longer be valid as the involved anionic vs. electronic carrier contributions cannot be separated. This accounts for the development of a comprehensive theory on carrier contribution and kinetics in memristive devices based on oxides with mixed anionic-electronic transport.

The development of high performance oxide-based memristive devices may be the cornerstone of the next generation of information storage devices replacing transistors or even allowing neuromorphic computing. Through our work we suggest new complimentary tools to probe the oxide materials characteristic diffusion coefficients, dominant carrier types and limiting currents on the example of mixed two-carrier conducting Pt|$SrTiO_{3-\delta}$|Pt bits. All of the latter material characteristics would not be accessible with state-of-the-art methodology of cyclic voltammetry and pulse experiments for memristors. However, these characteristics allow comparing and improving material selection and directly implicate field

strength requirements to optimize operation in the memristive regime towards enhanced performance specifications for valence-change memristive devices.

4. Experimental Section

Two-terminal cross-bar contacted Resistive Random Access Memory (ReRAM) switches were processed based on $SrTiO_3$ building block elements. The basic single device ReRAM elements were always composed of two platinum metal lines sandwiching a $SrTiO_3$ oxide element.

4.1. Thin Film Preparation of the ReRAM Device

The oxide-based ReRAM constituent $SrTiO_3$ was deposited on a randomly orientated single crystalline sapphire substrate with pre-structured Pt-bottom electrodes via pulsed laser deposition. For the pulsed laser deposition, own $SrTiO_3$ ceramic targets were synthesized by uniaxiallly and isostatically (88 MPa for 2 min) pressing and sintering of powder (Aldrich Chemistry, USA, ≥99.5%). Sintering conditions were an isothermal hold for 24 h at 1650 °C for a heating rate of 5 °Cmin^{-1} and cooling rate of 25 °C min^{-1}, respectively. The $SrTiO_3$ thin films were then deposited on round, randomly orientated, double side polished sapphire substrates (Stettler, Switzerland, Ø35 mm) by pulsed laser deposition (PLD, Surface Advanced PLD Technology, Germany; KrF excimer laser, 248 nm). A round metal mask with a 20 mm diameter hole was used to maintain access to the bottom electrodes. The deposition was carried out at 48 mJ per pulse at a repetition rate of 10 Hz with a substrate-to-target distance of 8.5 cm and under a constant oxygen flow with a background pressure of 0.0267 mbar at 700 °C. After reaching a background pressure of 4×10^{-6} mbar the substrate was heated up to the deposition temperature with a rate of 10 °C min^{-1}. 48000 and 29000 laser pulses were employed resulting in a film thickness of 620 nm and 740 nm analyzed via profilometer measurements Dektak XT Advanced profilometer (Bruker, Germany). Cubic phase of the thin film was confirmed by X-ray Diffraction (Bruker D8, $Cu_{K\alpha}$), see Supporting Information Figure S1.

4.2. ReRAM Device Fabrication

In the following we describe the device microfabrication route to shape the thin film constituents to single side- and cross-bar memristive ReRAM elements on the sapphire substrates. All steps of the device fabrication were carried out in an ISO class 4 cleanroom. Prior to the photolithography of the bottom electrodes the sapphire substrates were thoroughly cleaned for 3 minutes in an ultrasonic bath in acetone, isopropanol and water bath consecutively and then dried for 5 minutes on a hotplate at 110 °C. For micro patterning the bottom metal electrodes AZ nLOF 2070 (1:0.4) negative photoresist (Microchemicals, Germany) was used. The samples were spinned at a speed of 4750 RPM for 45 seconds, then softbaked at 110 °C for 180 seconds and afterwards rehydrated for at least 10 minutes. The samples were then aligned (Karl-Suss MJ3B mask aligner) and exposed through a custom made photolithography foil mask (Selba, Switzerland) to broadband ultraviolet light with a dose of 210 mJcm^{-2} and subsequently a post bake at 110 °C for 90 seconds was carried out. Finally the bottom electrode pattern was developed with MIF 726 developer for 90 seconds and rinsed in water. In a next step the samples were cleaned in an O_2 plasma asher (Technics Plasma TePla 100 asher system) for two minutes.

The thin film deposition of the *ReRAM metal electrode elements* was carried out by electron beam evaporation (Plassys MEB 550, France). The bottom metal electrodes consist of Ti 25 nm (adhesion layer) and Pt 100 nm. The remaining photoresist was then stripped off successively in DMSO, acetone and water. The top electrodes were fabricated alike after the pulsed laser deposition of the $SrTiO_3$ without adhesion layer.

4.3. Electrical Characterization of ReRAM Device Elements

All electrical measurements were carried out in a custom made closed high-vacuum microprobe station with a heating stage enabling a temperature range of RT-650 °C (Everbeing Taiwan and Electrochemical Materials ETH Zurich Switzerland) with Solatron impedance analyzer (SI 1287 Electrochemical Interface, SI 1260 Impedance Phase Analyzer). For contacting the microelectrodes tungsten and platinum tips were positioned via micro positioners employing a stereo light microscope (Nikon SMZ 1500).

In this study basically three types of electrical characterization were pursued as strategy: First, bias dependent conductivity measurements via temperature to study the Arrhenius like behavior of transport and defects involved. Rather unusual is that we applied a variation of positive and negative bias stress for activation energy measurements to correlate these findings later on to the ReRAM characteristics. Second, classic *ReRAM cyclic voltammetry* device measurements with respect to sweep rate for room temperature were undertaken. Third, the ReRAM elements were subjected to *chronoamperometry measurements*. In these titration experiments a constant bias stimulus is applied to a single ReRAM device element and the current response is studied over time.

For the first type of measurement namely the bias dependent conductivity measurements the samples were heated in the temperature range of 300–525 °C in 25 °C steps. After a minimum equilibration time of 10 minutes an averaged conductivity over 5 minutes was measured. The temperature was measured with a micro positioned K-type thermocouple positioned on top of the sample close to the measured top-electrode. The bias stimulus was varied from +100 mV to ±3 V for the Arrhenius measurements. Data analysis and fitting was undertaken with MATLAB.

The *ReRAM cyclic voltammetry* device measurements were carried out for a bias range of ±1 V to ±12 V to define reasonable SET and RESET bipolar voltages with ±4 V for sweep rates of 5–50 mVs^{-1} to prevent electrical breakdown. All bits were at least cycled 10 times as an initial electroforming step to set the bit in a stable state before any further electrical characterization was carried out analogue as reported in literature.[38,46,62,71] For testing reproducibility behavior always a minimum of 10 consequent cycles were measured up to 200 cycles.

For the *chronoamperometry* measurements first ten subsequent cycles with a SET and RESET voltage of ±4 V with a constant sweep rate of 50 mVs^{-1} were applied to equilibrate the system. Thereafter a first SET voltage with a positive polarity to the top electrode was applied for 120 minutes and the current measured before the sample was set into its low resistance state again by applying the RESET voltage for an hour. The SET and RESET voltages were either increased or decreased by 0.1 V steps in a bias range of 1.0 V to 4.0 V.

4.4. Chemical and Structural Characterization

After the electrical characterization one sample was cleaved and 5 nm platinum was sputtered to record top- and cross-view scanning electron microscope images (SEM, LEO 1530, Zeiss). All thin film samples and PLD targets were characterized by X-ray Diffraction (Bruker D8) at a Cu K_α wavelength.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author. Section 1 presents the XRD pattern of the used $SrTiO_{3-\delta}$ thin film sample. Section 2 shows maximum conductivity change during 200 cycles in cyclic voltammetry experiments.

Acknowledgements

The authors thank J. Aeschlimann for support with electrochemical measurements, and Prof. R. Nesper and Dr. M. Wörle for the use of the XRD facility. Funding of this project was supported by the Swiss National Science Foundation Projects 138914 and 144988 and is gratefully acknowledged.

Received: July 10, 2014
Revised: August 28, 2014
Published online: September 25, 2014

[1] International Technology Roadmap for Semiconductor Industry 2013(ITRS), http://www.itrs.net/, accessed February 14, 2014.
[2] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2009**, *459*, 80.
[3] J. J. Yang, M. D. Pickett, X. M. Li, D. A. A. Ohlberg, D. R. Stewart, R. S. Williams, *Nat. Nanotechnol.* **2008**, *3*, 429.
[4] L. O. Chua, *IEEE Trans. Circuits Syst.* **1971**, *Ct18*, 507.
[5] Y. Li, S. Long, Q. Liu, H. Lü, S. Liu, M. Liu, *Chinese Sci. Bull.* **2011**, *56*, 3072.
[6] J. L. M. Rupp, P. Reinhard, D. Pergolesi, T. Ryll, R. Tolke, E. Traversa, *Appl. Phys. Lett.* **2012**, *100*, 012101.
[7] Rainer Bruchhaus, R. Waser, *Thin Film Metal-Oxides* Springer, **2010**, 131.
[8] Y. V. Pershin, M. Di Ventra, *Adv. Phys.* **2011**, *60*, 145.
[9] A. A. Felix, J. L. M. Rupp, J. A. Varela, M. O. Orlandi, *J. Appl. Phys.* **2012**, *112*, 054512.
[10] R. Muenstermann, T. Menke, R. Dittmann, R. Waser, *Adv Mater* **2010**, *22*, 4819.
[11] J. Yao, L. Zhong, D. Natelson, J. M. Tour, *Sci. Rep.* **2012**, *2*, 242.
[12] C. Yoshida, K. Tsunoda, H. Noshiro, Y. Sugiyama, *Appl. Phys. Lett.* **2007**, *91*, 223510.
[13] M. J. Lee, C. B. Lee, D. Lee, S. R. Lee, M. Chang, J. H. Hur, Y. B. Kim, C. J. Kim, D. H. Seo, S. Seo, U. I. Chung, I. K. Yoo, K. Kim, *Nat. Mater.* **2011**, *10*, 625.
[14] H. Y. Lee, Y. S. Chen, P. S. Chen, P. Y. Gu, Y. Y. Hsu, S. M. Wang, W. H. Liu, C. H. Tsai, S. S. Sheu, P. C. Chiang, W. P. Lin, C. H. Lin, W. S. Chen, F. T. Chen, C. H. Lien, M. J. Tsai, *IEEE Int. Electron Devices Meeting* **2010**, 460.
[15] S. Tappertzhofen, H. Mundelein, I. Valov, R. Waser, *Nanoscale* **2012**, *4*, 3040.
[16] B. Reihl, J. G. Bednorz, K. A. Muller, Y. Jugnet, G. Landgren, J. F. Morar, *Phys. Rev. B* **1984**, *30*, 803.
[17] R. Waser, R. Dittmann, G. Staikov, K. Szot, *Adv. Mater.* **2009**, *21*, 2632.
[18] A. Rothschild, W. Menesklou, H. L. Tuller, E. Ivers-Tiffee, *Chem. Mater.* **2006**, *18*, 3651.
[19] I. Denk, W. Münch, J. Maier, *J. Am. Ceram. Soc.* **1995**, *78*, 3265.
[20] R. A. De Souza, V. Metlenko, D. Park, T. E. Weirich, *Phys. Rev. B* **2012**, 85.
[21] R. Merkle, J. Maier, *Angew. Chem. Int. Ed.* **2008**, *47*, 3874.
[22] F. Aguesse, A. K. Axelsson, P. Reinhard, V. Tileli, J. L. M. Rupp, N. M. Alford, *Thin Solid Films* **2013**, *539*, 384.
[23] I. Denk, J. Claus, J. Maier, *J. Electrochem. Soc.* **1997**, *144*, 3526.
[24] P. Lupetin, G. Gregori, J. Maier, *Angew. Chem. Int. Ed.* **2010**, *49*, 10123.
[25] G. Gregori, P. Lupetin, J. Maier, *Ionic Mixed Cond. Ceram.* **2012**, *45*, 19.
[26] C. Ohly, S. Hoffmann-Eifert, X. Guo, J. Schubert, R. Waser, *J. Am. Ceram. Soc.* **2006**, *89*, 2845.
[27] M. Schie, A. Marchewka, T. Muller, R. A. De Souza, R. Waser, *J. Phys.-Condens. Mat.* **2012**, *24*, 485002.
[28] R. A. De Souza, J. Fleig, J. Maier, O. Kienzle, Z. Zhang, W. Sigle, M. Rühle, *J. Am. Ceram. Soc.* **2003**, *86*, 922.
[29] J. L. M. Rupp, B. Scherrer, N. Schauble, L. J. Gauckler, *Adv. Funct. Mater.* **2010**, *20*, 2807.
[30] J. L. M. Rupp, B. Scherrer, L. J. Gauckler, *Phys. Chem. Chem. Phys.* **2010**, *12*, 11114.
[31] B. Scherrer, S. Heiroth, R. Hafner, J. Martynczuk, A. Bieberle-Hutter, J. L. M. Rupp, L. J. Gauckler, *Adv. Funct. Mater.* **2011**, *21*, 3967.
[32] B. Yildiz, *MRS Bull.* **2014**, *39*, 147.
[33] J. L. M. Rupp, *Solid State Ionics* **2012**, *207*, 1.
[34] S. Schweiger, M. J. Kubicek, F. Messerschmitt, C. Murer, J. L. Rupp, *ACS Nano* **2014**, *8*, 5032.
[35] S. Schweiger, F. Messerschmitt, J. L. M. Rupp, (ETH Zurich), Patent Application PCT/EP2014/001020, EU, **2013**.
[36] X. Guo, *Appl. Phys. Lett.* **2012**, *101*, 152903.
[37] S. Menzel, M. Waters, A. Marchewka, U. Bottger, R. Dittmann, R. Waser, *Adv. Funct. Mater.* **2011**, *21*, 4487.
[38] X. W. Sun, G. Q. Li, L. Chen, Z. H. Shi, W. F. Zhang, *Nanoscale Res. Lett.* **2011**, *6*, 599.
[39] R. Oligschlaeger, R. Waser, R. Meyer, S. Karthauser, R. Dittmann, *Appl. Phys. Lett.* **2006**, *88*, 042901.
[40] C. Park, Y. Seo, J. Jung, D.-W. Kim, *J. Appl. Phys.* **2008**, *103*, 054106.
[41] S. Saraf, M. Markovich, T. Vincent, R. Rechter, A. Rothschild, *Appl. Phys. Lett.* **2013**, *102*, 022902.
[42] D. J. Seong, M. Jo, D. Lee, H. Hwang, *Electrochem. Solid. St.* **2007**, *10*, H168.
[43] D. Sacchetto, P. E. Gaillardon, M. Zervas, S. Carrara, G. De Micheli, Y. Leblebici, *IEEE Circ. Syst. Mag.* **2013**, *13*, 23.
[44] P. E. Gaillardon, D. Sacchetto, G. B. Beneventi, M. H. Ben Jamaa, L. Perniola, F. Clermidy, I. O'Connor, G. De Micheli, *IEEE Trans. Nanotechnol.* **2013**, *12*, 40.
[45] A. Sawa, *Mater. Today* **2008**, *11*, 28.
[46] M. Janousch, G. I. Meijer, U. Staub, B. Delley, S. F. Karg, B. P. Andreasson, *Adv. Mater.* **2007**, *19*, 2232.
[47] T. Menke, R. Dittmann, P. Meuffels, K. Szot, R. Waser, *J. Appl. Phys.* **2009**, *106*, 114507.
[48] K. Szot, W. Speier, G. Bihlmayer, R. Waser, *Nat. Mater.* **2006**, *5*, 312.
[49] C. Rodenbucher, W. Speier, G. Bihlmayer, U. Breuer, R. Waser, K. Szot, *N. J. Phys.* **2013**, *15*, 03017.
[50] A. Leshem, E. Gonen, I. Riess, *Nanotechnology* **2011**, *22*, 254024.
[51] D. Kalaev, I. Riess, *Solid State Ionics* **2013**, *241*, 17.
[52] I. R. D. Kalaev, *Solid State Ionics* **2014**, *262*, 883.
[53] D. B. Strukov, G. S. Snider, D. R. Stewart, R. S. Williams, *Nature* **2008**, *453*, 80.
[54] J. E. B. Randles, *Trans. Faraday Soc.* **1948**, *44*, 327.
[55] A. J. Bard, L. R. Faulkner, *Electrochemical Methods. Fundamentals and Applications* Ch. 2, Wiley, New York, USA, **2001**.
[56] W. Wu, G. Y. Jung, D. L. Olynick, J. Straznicky, Z. Li, X. Li, D. A. A. Ohlberg, Y. Chen, S. Y. Wang, J. A. Liddle, W. M. Tong, R. S. Williams, *Appl. Phys. A-Mater.* **2005**, *80*, 1173.
[57] T. Raja, S. Mourad, *2009 Int. Conf. Commun. Circ. Syst. Proc.* **2009**, *1–2*, 939.
[58] Y. A. Abramov, V. G. Tsirelson, V. E. Zavodnik, S. A. Ivanov, I. D. Brown, *Acta Crystallogr. B* **1995**, *51*, 942.
[59] P. Plonczak, A. Bieberle-Hutter, M. Sogaard, T. Ryll, J. Martynczuk, P. V. Hendriksen, L. J. Gauckler, *Adv. Funct. Mater.* **2011**, *21*, 2764.
[60] S. Tappertzhofen, I. Valov, T. Tsuruoka, T. Hasegawa, R. Waser, M. Aono, *ACS Nano* **2013**, *7*, 6396.
[61] T. Liu, Y. H. Kang, S. El-Helw, T. Potnis, M. Orlowski, *Jpn. J. Appl. Phys.* **2013**, *52*, 084202.
[62] J. W. Park, M. K. Yang, K. Jung, J. K. Lee, *IEEE Trans. Electron Dev.* **2008**, *55*, 1782.
[63] U. Balachandran, N. G. Eror, *J. Solid State Chem.* **1981**, *39*, 351.

[64] E. J. Tarsa, E. A. Hachfeld, F. T. Quinlan, J. S. Speck, M. Eddy, *Appl. Phys. Lett.* **1996**, *68*, 490.
[65] R. T. Thomas, *J. Phys. D Appl. Phys.* **1970**, *3*, 1434.
[66] G. A. Cox, R. H. Tredgold, *Br. J. Appl. Phys.* **1965**, *16*, 427.
[67] E. Deiss, *Electrochim. Acta* **2002**, *47*, 4027.
[68] A. Hackmann, O. Kanert, *Radiat. Eff. Defect Solids* **1991**, *119*, 651.
[69] D. B. Schwarz, H. U. Anderson, *J. Electrochem. Soc* **1975**, *122*, 707.
[70] I. Denk, W. Munch, J. Maier, *J. Am. Ceram. Soc* **1995**, *78*, 3265.
[71] S. Hirose, H. Niimi, K. Kageyama, A. Ando, H. Ieki, T. Omata, *Jpn. J. Appl. Phys.* **2013**, *52*, 045802.